ME-914

project
mercury

HANDBOOK OF INSTRUCTIONS
FOR
TRANSFER REGISTER
MEC MODEL 79

prepared for
National Aeronautics and Space Administration
Contract No. NAS 1-430

31 December 1960
Revised 18 October, 1961

Milgo Electronic Corporation
for
International Business Machines Corporation

in association with,

WESTERN ELECTRIC COMPANY, INC.

LIST OF EFFECTIVE PAGES

TOTAL NUMBER OF PAGES IS 138, AS FOLLOWS:

Page No.	Issue
*Title Page	18 October 61
*A Page	18 October 61
i	Original
ii	Blank
iii	Original
iv	Blank
v	Original
vi	Original
1-1 thru 1-2	Original
*2-1	30 July 61
*2-2	30 July 61
3-1 thru 3-2	Original
*3-3	30 July 61
3-4	Original
*3-5	30 July 61
3-6	Original
*3-7	30 July 61
3-8 thru 3-11	Original
3-12	Blank
4-1 thru 4-2	Original
5-1 thru 5-3	Original
5-4	Blank
6-1	Original
6-2	Blank
7-1 thru 7-2	Original
*7-3	30 July 61
7-4	Original
*7-5	30 July 61
7-6 thru 7-13	Original
7-14	Blank
8-1	Original
8-2	Blank
Wire List	
27 Pages	Original
1 Page	Blank
9-1	Original
9-2	Blank
*9-3	30 July 61
9-4	Blank
*9-5	30 July 61
9-6	Blank
*9-7	30 July 61
9-8	Blank
9-9	Original
9-10	Blank
9-11	Original
9-12	Blank
9-13	Original
9-14	Blank
9-15	Original
9-16	Blank
Appendix	
Title Page	Original
Page 1 of 5 thru 5 of 5	Original
Page 1 of 7 thru 7 of 7	Original
Page 1 of 3 thru 3 of 3	Original
Page 1 of 3 thru 3 of 3	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 3 thru 3 of 3	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 3 thru 3 of 3	Original
Page 1 of 3 thru 3 of 3	Original
Page 1 of 2 thru 2 of 2	Original
Page 1 of 8 thru 8 of 8	Original

* The asterisk indicates pages changed, added or deleted by the current change.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

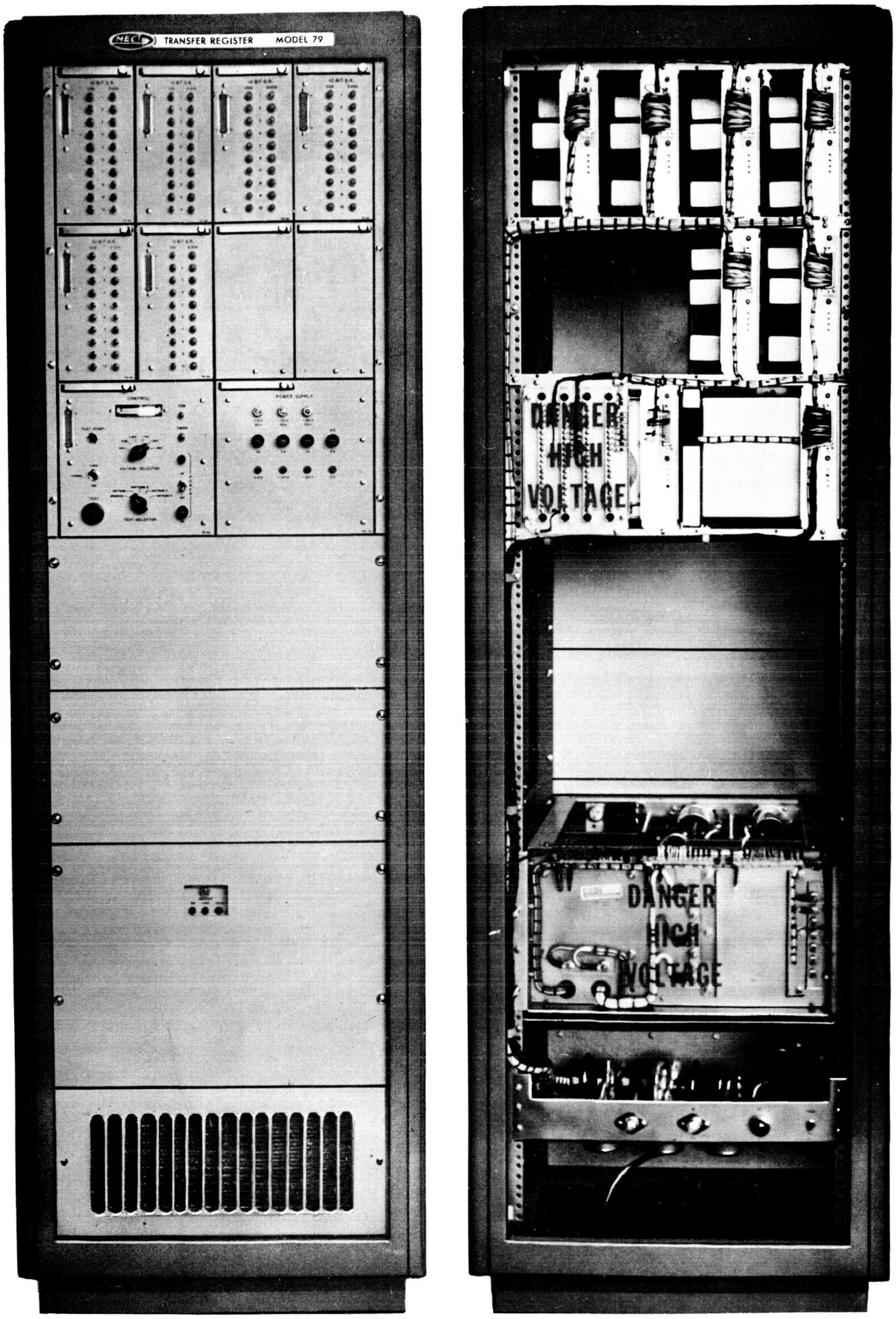


Figure 1-1. MEC Model 79 Transfer Register

CHAPTER I
INTRODUCTION

1-1. PURPOSE OF THE EQUIPMENT

1-1.1. The Milgo Electronic Corporation (MEC) Model 79 Transfer Register receives the serial data output from a Computer and converts this data into two groups of parallel digital outputs:

a. "even" output

b. "odd" output

1-1.1.1. The "even" outputs provide a continuous readout except for a brief time (approximately 50 microseconds). During this brief period, new data is inserted into the flip-flops. This data is renewed every other frame of input data.

1-1.1.2. The "odd" outputs operate like the "even" except they are renewed on alternate input data frames.

1-1.2. The Transfer Register accepts the last 56 data bits from a 96 bit word. The first 40 bits are fed through the Transfer Register to the serial output of the Transfer Register. The 40 bits are then fed to a MEC Model 1576 D-A Converter. The transfer Register also uses the controlled signals furnished by the Computer to facilitate the control of the flow of the data. "Select and ready" and "sample" are controlled signals. Outputs are provided for the D-A Converter so that the control signals, such as "select and ready" and "sample", are obtained from the Transfer Register. These control signals control the data flow in the D-A Converter.

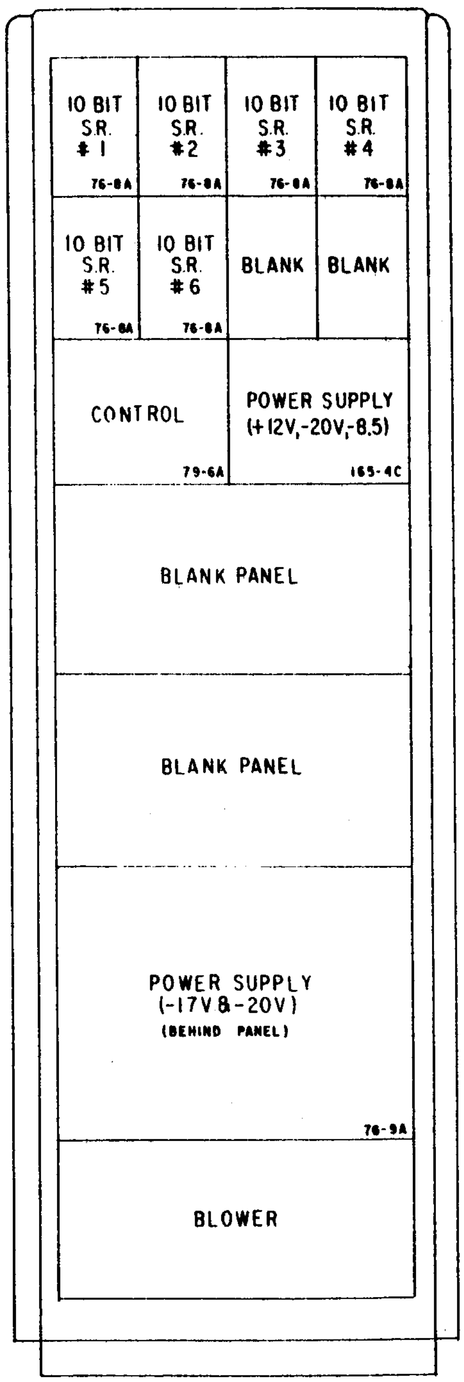
1-1.3. Bits #41 and #42 are the first two bits which are used with the Transfer Register. These bits determine whether the input data frame was an "odd" frame or an "even" frame. If the input data is an "even" frame of data, the parallel output will be made available on the "even" outputs. If the input data is on "odd" frame of data, the outputs will be made available on the "odd" outputs. In normal operation, alternate input frames will be "even" and "odd" alternately. Both the "even" outputs and the "odd" outputs are brought out to the connector plugs on the rear panel of the rack. This facilitates the connection of external digital equipment to them. Each output has the ability to furnish 200 milliamperes at -17 volts, for a "1" and is at 0 volts for a "0".

1-2. SCOPE OF THE MANUAL

This instruction manual describes the MEC Model 79 Transfer Register, designed and manufactured by MEC, for International Business Machines, Federal Systems Division, Kingston, New York, in conjunction with Project Mercury.

1-3. PURPOSE OF THE MANUAL

This instruction manual is provided as an aid to better understanding of the operation and theory of the MEC Model 79 Transfer Register and its associated equipment. It offers a complete technical explanation coupled with applicable illustrations. It is necessary that the operator, or any person involved in the operation of this equipment, thoroughly read and understand the contents of this manual.



*contains plug-in modification

Figure 1-2. Chassis Arrangement

CHAPTER II

GENERAL DESCRIPTION

2-1. PHYSICAL DESCRIPTION

The Transfer Register is housed in a single relay rack approximately 24" wide, 22" deep, and 74" high. Its weight is approximately 625 pounds. All chassis are of modular construction and employ 50 pin connectors for the connection of each chassis to the rack wiring. The location of each chassis is illustrated in figure 1-2. The top two rows house the six MEC Model 76-8A 10 Bit Shift Registers in which the parallel data is readout. The next row houses the MEC Model 79-6A Control Chassis and the MEC Model 165-4C Power Supply. Just above the Blower (on the bottom) a -17 volt and -20 volt Power Supply is housed and is bolted to the main frame of the rack. The Blower is a two speed blower, capable of delivering 500 cubic feet of filtered room air per minute for internal cooling of the Transfer Register rack. The Blower should be operated at high speed at all times during the operation of this equipment. In the lower rear of the rack is a mounting bracket in which all input and output connectors are located. The input ac fuses and safety ac power switch are located on the same panel.

2-2. ELECTRICAL REQUIREMENTS

The Transfer Register operates from a single phase 115 vac ± 10 volts, 60 cycle, ± 5 cycles system. The input current is 15 amperes.

2-3. DATA INPUTS

Connector J20 provides the necessary inputs from the Computer. There are three input lines to the Transfer Register from the Computer: "select and ready" line, "sample" pulse line, and the "data" line. The "select and ready" line is a control signal in which the Computer signifies to the Transfer Register that it has data to present. A return signal from the Transfer Register called the "D-A and transfer register ready" (D/A - T/R ready) signal informs the Computer that the Transfer Register and the attached D-A Converter is prepared to read the next bit of data. The data input to this Transfer Register consists of 96 bits of serial data which are transmitted over the data input line from the Digital Computer. Each time a new data bit is presented to the input data lines and the "D-A ready" signal indicates that the D-A Converter is prepared to read the new bit of data, a "sample" pulse is sent to the D-A Converter from the Computer. There must be a "D/A-T/R ready" and a "sample" pulse for each bit of data received from the Computer. A significant bit or a "1" level on any one of these three lines from the Computer will be +8 volts ±2 volts. A non-significant or "0" level from the computer is 0 volts ±.5 volts.

2-4. OUTPUT SIGNALS

2-4.1. Output Signals to the D-A Converter - There is an auxiliary output from the Transfer Register for the operation of a D-A Converter (such as, MEC Model 1576 D-A Converter). Connector J16 furnishes the necessary outputs for the operation of the D-A Converter. The outputs to the D-A are: "data for the D-A", "select and ready to the D-A", and "sample to the D-A". A return pulse from the D-A called "D-A ready" is provided for the operation of the combined system. Refer to manual ME-916 for details on the requirements for the operation of the MEC Model 1576 D-A Converter.

2-4.2. Parallel Digital Data Outputs - Connectors J17, J18 and J19 provide the parallel data outputs for the Transfer Register. As will be described in the Theory of Operation (Chapter 3) there are "odd" outputs and "even" outputs; each is provided to the output connectors. Each output has the capacity of driving a load of 200 milliamps at -17 volts for a "1" (a "0" is 0 volts).

2-4.3. Connector J21 provides a timing output which is the contact closure of a relay when bit #41 is detected and put into storage in the Transfer Register. At this particular time, the contacts of the timing signal will open for approximately 20 milliseconds.

2-5. POWER INPUT CONNECTIONS

The input ac power is to be connected to the Transfer Register rack by means of an MS connector to J15, as found in the lower rear of the rack. The input requirements are 115 volts ±10 volts a-c single phase, 60 cycles, ±5 cycles at 15 amperes. The input is connected to terminals A and C of J15 (Table 5-1).

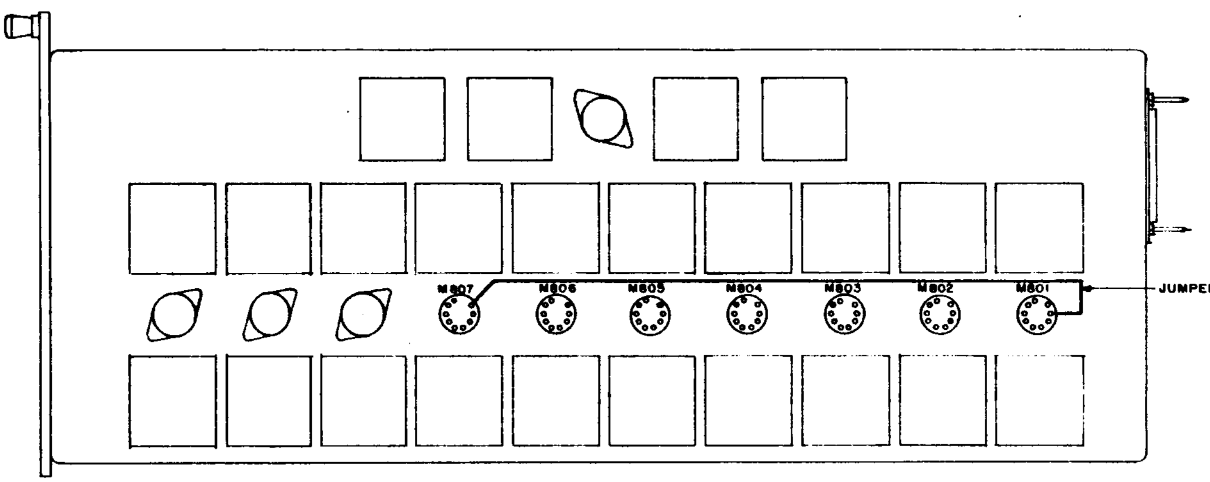


Figure 2-1. Plug-in Modification

CHAPTER III

THEORY OF OPERATION

3-1. General

3-1.1. Digital data bits are received by the Transfer Register through the digital input plug, J20, which is located at the rear of the base of the Transfer Register rack. Along with the data input there are three control signals which are used so that this data may be properly brought into the Transfer Register. These signals are a "select and ready" input (provided by the Computer to signify that the Computer has data available), a "sample" input (a signal generated by the Computer to signify that the new data bit has been presented on the data line), and a "D/A-T/R ready" (generated by the Transfer Register so that it can signify to the Computer that it is also ready to receive the next data bit). As shown on the timing diagram of the Computer control signals in figure 3-1, there are a few requirements on the timing of the "data", "sample", "select and ready" and "D/A-T/R ready" signals.

3-1.2. Timing Requirements - There are a total of N plus 1 "D/A-T/R ready" signals (N = the number of input data bits) provided by the Transfer Register. In this instance, there would be a total of 97 pulses. The timing between these pulses is determined by the Control Chassis and is approximately 250 microseconds. The "select and ready" will remain up (+8 volts) during the complete time in which the data is being provided. As shown in figure 3-1 there is a minimum and maximum timing between the "data", "D/A-T/R ready", and the "sample" pulses. These minimums and maximums must be maintained for proper operation of the system.

3-1.3. There are a total of 96 serial input data bits which are received through the Control Chassis. These bits are shifted through six 10 Bit Shift Registers in series and a MEC Model 1576 D-A Converter, giving a total capacity of 56 serial bits of information in the Transfer Register (the remaining 40 bits are in the D-A Converter). The shifting and controlling of these data bits is accomplished by the operation of the Control Chassis. This operation is described in paragraph 3-2 on the Control Chassis.

3-1.4. The "sample" input is used to tell the Control Chassis that a new data bit is available and should be received into the cores. After the last data bit has been received and sampled, the last "D/A-T/R ready" will go out to the Computer to signify to the Computer that the complete word has been received. Then the Computer will drop the "select and ready" line which will have been at a +8 volt d-c level for approximately 25 milliseconds. This time is determined by the accuracy of the 250 microsecond interval between each "D/A-T/R ready" pulse.

3-1.5. When the last 56 serial bits of data have been put into storage in the cores found in the six 10 Bit Shift Registers, a pulse is generated by the fall of "select and ready" which produces the necessary pulses to parallel transfer this data into transistorized flip-flops.

3-1.6. In normal operation, one new data frame will be received every 500 milliseconds.

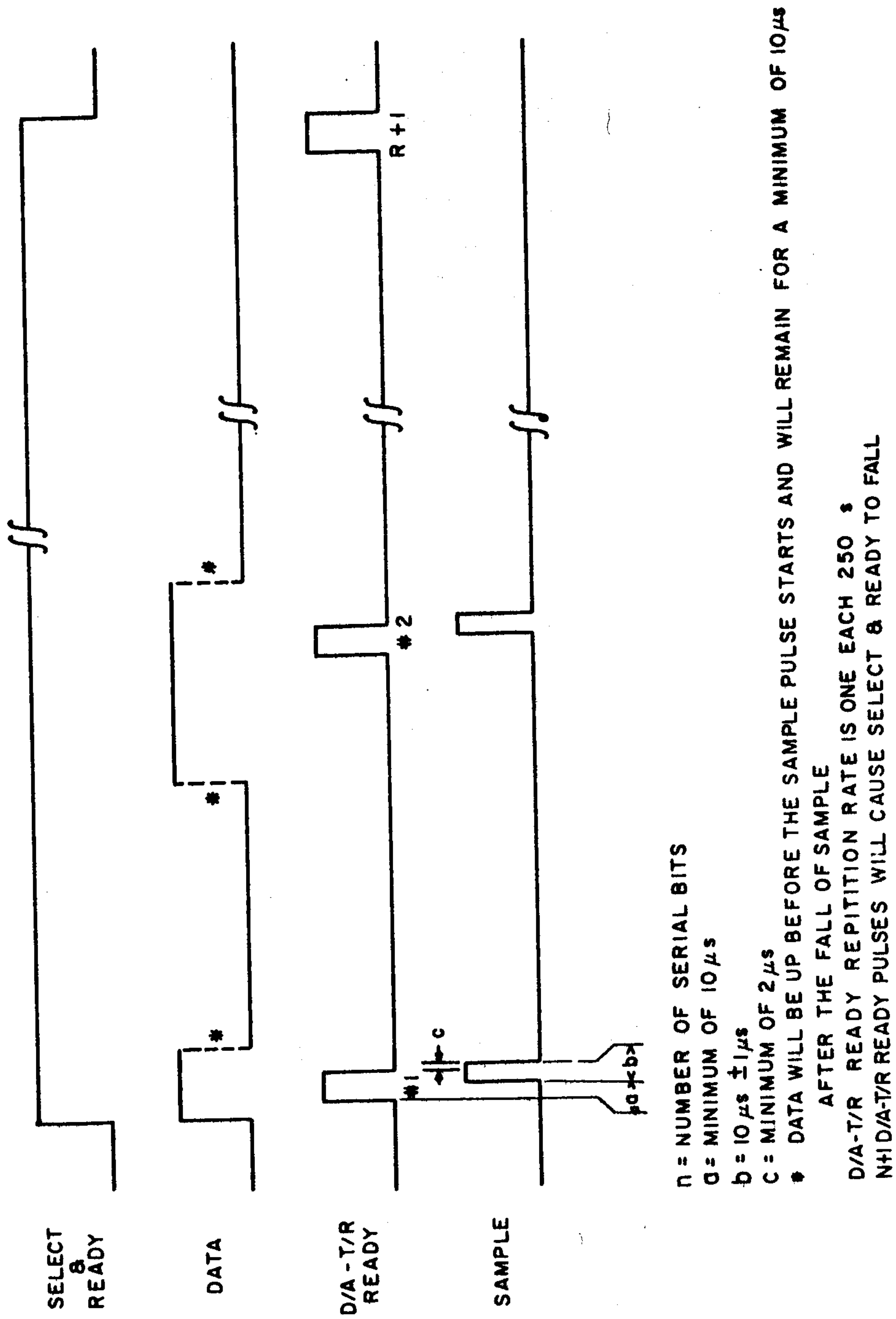


Figure 3-1. Computer Control Signals

3-2. CONTROL CHASSIS, MEC Model 79-6A (Figures 9-2 and 9-3)

3-2.1. Functions - The Control Chassis is used for the purpose of receiving the data and control signals from the Computer, detecting these signals, and then using these signals for controlling the data flow throughout the Transfer Register. A secondary function of the Control Chassis is to furnish control signals and data for the operation of a MEC Model 1576 D-A Converter which may be connected to the serial outputs of the Transfer Register.

3-2.2. When "select and ready" goes from 0 volts to +8 volts being a "1", it goes through resistor R603 to pulse amplifier N601A, producing a negative pulse. "Select and ready" also goes through resistor R622 to the input of pulse amplifier N608A. The output of pulse amplifier N608A goes through pulse amplifier N608B, producing a positive pulse from 0 to +8 volts. This positive pulse goes out through the outside of the rack as the "select and ready" output to the D-A Converter. This particular "select and ready" is the "select and ready" which the D-A Converter will consider the same as a direct connection to the Computer. The output of the first pulse amplifier (N601A) has three separate outputs. One goes through pulse amplifier N601B, which produces a pulse from -20 volts to 0 volts. The second output (through diode CR601) and the third output (through capacitor C665 and diode CR655) are used only when the "select and ready" input from the computer falls back to a "0" (0 volts) and therefore will be considered at that time.

3-2.3. The output from pulse amplifier N601B is used for the operation of several "AND" gates. These "AND" gates are used in order to develop "D/A-T/R ready". The output of pulse amplifier N601B, which is a positive going pulse when "select and ready" went to a "1", provides the inputs of two "AND" gates. The first "AND" gate consists of capacitor C619, with resistors R629 and R630 associated with diode CR613 which provides one of the pin 6 inputs to turn on the flip-flop N610. Since this "AND" gate is normally open and would be open at this time, this will trigger flip-flop N610 to the "1" condition. The pin 8 output of flip-flop N610 goes to the one of the inputs of a three input "AND" gate, consisting of diodes CR617, CR618, and CR619. One of the other inputs of this "AND" gate is the output of pulse amplifier N601B, which is also a "1" at this time. The third

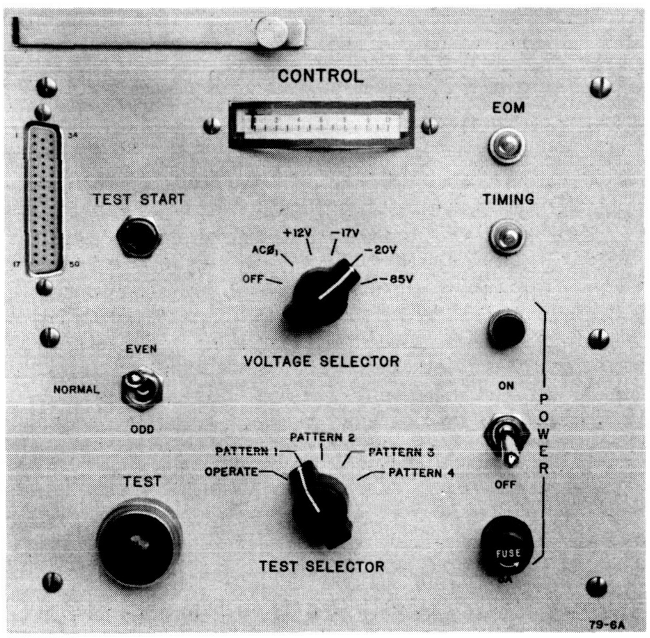


Figure 3-2. Control Chassis

input being on pin 7 output of one-shot N633 which is in the "1" (0 volts) condition at this time, since it has not been triggered. Therefore, this "AND" gate is open and will produce a pulse through emitter follower N611B which produces the first "D/A-T/R ready" signal to the Computer.

3-2.4. Upon receipt of the "D/A-T/R ready" signal by the Computer, the Computer will furnish the first "sample" pulse to the Transfer Register. This pulse is received through pin 5 of the input plug to the Control Chassis and goes to switch S601B, providing that an "AND" gate, consisting of diodes CR622 and CR623, is open. Since "select and ready" is a "1", this "AND" gate is open and "sample" will trigger pulse amplifier N612A producing a negative pulse (from 0 volts to -20 volts). This negative pulse triggers pulse amplifier N612B, producing a positive pulse (-20 volts to 0 volts - a "0" is -20 volts and a "1" is 0 volts). The output of pulse amplifier N612B goes to two places; first it triggers one-shot N613 through capacitor C623 and second it provides one of the inputs for the "AND" gate for the triggering of flip-flop N616. This "AND" gate consists of diodes CR625 and CR627. During the same time in which a "sample" pulse was received, there was data available on the data line which goes through switch S601A resistor R619 and emitter follower N611, which then produces the second input to the above mentioned "AND" gate. If both conditions are "1"s, i.e., if "sample" pulse is received and data is a "1" (+10 volts), then flip-flop N616 is set to the "1" condition. As previously described, one-shot N613 was triggered at this same time and produced two pulses; a 10 microsecond delayed pulse on pin 5 in which the positive going edge of the negative pulse will trigger a 70 microsecond one-shot N614. The positive going pulse of one-shot N613 triggers pin 7 of flip-flop N610 through diode CR656, turning it back to the "0" condition. Then in 80 microseconds, as determined by the total delay of one-shots N613 and N614, the pin 5 output of one-shot N614 will trigger one-shot N609. The pin 5 (180 microseconds delay) output of one-shot N609 will pass through the "AND" gate consisting of capacitor C617, resistor R626 and R627, and then go through diode CR612 and trigger flip-flop N610 to a "1". This produces the next "D/A-T/R ready" signal for the Computer. This signal has been generated in approximately 260 microseconds after the first one had been generated by "select and ready".

3-2.5. The pin 7 output of one-shot N614, which was delayed a total of 10 microseconds from the time in which "sample" was received, triggers core driver N615. Core driver N615 is basically a power amplifier which is used as both a core drive trigger for the six 10 Bit Shift Registers, found within the rack of equipment, and also drives the three cores M602, M603 and M604 found in this chassis. Upon the receipt of "sample", flip-flop N616 was triggered to the "1" state, provided that a data "1" was on the data line. If flip-flop N616 was in the "1" condition, it will be triggered to the "0" condition in approximately 80 microseconds after it was triggered to the "1" condition. This pulse comes from the delayed output (pin 5) of one-shot N614. If this action takes place, the positive going pulse produced on pin 5 of flip-flop N616 triggers one-shot N617, through capacitor C630. This produces a positive going pulse on the pin 7 output of one-shot N617 and inserts a "1" into the first core in 10 Bit Shift Register #1 which is the modified 10 Bit Shift Register (figure 1-2). This process is repeated each time a "D/A-T/R ready" is sent to the Computer, thus producing a "sample" pulse. This process is repeated for the total number of data pulses (96) in which the Computer will give the Transfer Register. It will be noted, that since "select and ready" produced the first "D/A-T/R ready", and "sample" pulse produced the rest of them, there will be a total of one more "D/A-T/R ready" than there are "sample" pulses. The Computer will use the last one of these "D/A-T/R ready" signals as a disconnect signal, so that it will drop its "select and ready" line until a new batch of data is made available. The new data will be made available at the rate of one frame each 500 milliseconds.

3-2.6. Since the MEC Model 1576 D-A Converter is used in conjunction with the Transfer Register and it also must be ready to receive new data, it will produce a

"D-A ready" in order that the "D/A-T/R ready" be provided. The "D-A ready" from the D-A Converter will enter pin 24 of this chassis and trigger one-shot N633 to the "0" condition. This circuit works as follows. The positive going output of one-shot N609, which has been delayed exactly 80 microseconds from the time in which the first "sample" pulse was received, triggers one-shot N633 through capacitor C611 to the "1" condition. This produces a negative pulse on pin 7 of one-shot N633 and closes the "AND" gate in which one input is diode CR618. This "AND" gate will remain closed until one of two things happen:

a. when a "D-A ready" is received from the D-A Converter this will turn off one-shot N633 (a one-shot in which the time can be shorted by a secondary input as described in detail in the write-up in the appendix, on TN158). At this time, the output of pin 7 will return to 0 volts (a "1") and thus opening the "AND" gate so that the "D/A-T/R ready" may be presented.

b. if a "D-A ready" is not received by the Transfer Register in 500 microseconds, this one-shot will time out and open the "AND" gate. A "D/A-T/R ready" will be generated whether a "D-A ready" was received or not.

3-2.7. When "select and ready" falls to the "0" condition, which means that the last bit of data has been received, a negative going pulse goes through pulse amplifier N601A producing a positive pulse at its output. This positive pulse performs two functions. First, it passes through capacitor C665 and diode CR655 and resets flip-flop N610 to the "0" state, thus removing one of the inputs to the "AND" gate composed of diodes CR617, CR618, and CR619. The closing of this "AND" gate removes the input to pin 7 of N611B which in turn prevents any "D/A & T/R Ready" signal being sent to the computer. The second function performed by the positive pulse output of N601A is to trigger the 600 microsecond one-shot N602 by passing through the CR601 diode. The delayed output (pin 5) of N602 will trigger one-shot N604 or N606, provided the input to an "AND" gate (consisting of diode CR602 and resistors R607 and R608 with capacitor C603, or an "AND" gate consisting of diode CR605, resistors R612 and R611 and capacitor C607) is open by their respective input signals to diode CR602 or CR605. In normal operation, only one of these two "AND" gates will be open, as will be discussed later when the operation of the EVEN-ODD gates is considered. At this time, it will be assumed that one or the other of these two "AND" gates will be open, but not both. At the end of this 600 microseconds, one or the other of the one-shots N604 or N606 will be triggered. If one-shot N604 is triggered, it produces a positive pulse for 50 microseconds ("even reset trigger"), which is fed to all Shift Registers. It also triggers a 100 microsecond one-shot N605, which produces a 100 microsecond pulse "even gate". The "even reset trigger" pulse and "even gate" pulse are described as to their use in the operation of the Shift Registers in paragraph 3-3 on the operation of the 10 Bit Shift Registers. If the other "AND" gate was open as previously described, then one-shots N606 would be triggered. These one-shots produce a 50 microseconds pulse which is called "odd reset trigger" and triggers one-shot N607, producing a 100 microsecond pulse called "odd gate" The use of these two pulses is identical to the two previously described. Briefly, since either the "even" set or "odd" set of pulses will be generated, this will do the necessary gating in the Shift Registers so that the data is made available to the parallel readout in either the "even" flip-flops or the "odd" flip-flops.

3-2.8. Magnetic cores M602, M603 and M604 form the last three cores of the Shift Register, consisting of the six 10 Bit Shift Registers and these three cores. Shift Register #1 has been shortened and actually consists of only three cores. Therefore, the total length of the complete system is 56 cores and therefore can store a total of 56 data bits.

3-2.9. The operation of these three cores, along with their associated networks N618 through N625, operate in the following manner. The pin #4 output of core M603 triggers one-shot N624 each time a "1" is present in this core. The operation continues through the whole shifting of data and this is the path in which the data will flow to the D-A Converter which is on the end of the Transfer Register. The delayed output of 120 microseconds one-shot N624 triggers flip-flop N625 to the "1" condition, if there was a "1" in the core M603. The output of one-shot N609, being delayed 80 microseconds after the receipt of "sample" and of "data", triggers flip-flop N625 to the "0" condition. This flip-flop will change states at the rate of being a "1" for 40 microseconds and a "0" for the rest of the time (approximately 220 microseconds for all "1"s or until the next "1" is detected). The output of this flip-flop N625 will produce a pulse between 0 volts and +8 volts on pin 22 of plug P601 which is wired to an output jack on the rack. This furnishes the data input for the D-A Converter. As data is being shifted through cores M602 through M604, the states of the flip-flops N618, N619, N620 and N621 are not being changed except during the time in which either the "odd reset" and "odd gate" or the "even reset" and "even gate". These pulses are generated by the "AND" output of the fall of "select and ready" and the output of flip-flops N622 and N623, which are the two flip-flops which decide whether the data is an "even" frame or an "odd" frame of data. The ODD-EVEN information is provided by data #41 and #42.

3-2.10. As the data is being shifted through the cores, the pin 4 outputs of cores M602 and M603 are triggering pin 3 ("1" input) of flip-flops N622 and N623. Also, the pin 8 outputs of M602 and M603 are triggering the "0" inputs (pin 7) to the opposite flip-flop. The pin 4 output of core M602 is triggering the "1" input of flip-flop N622 and its pin 9 output is triggering the "0" side of flip-flop N623. The pin 4 output of the core is a 6 microsecond pulse; the pin 9 output is a 40 microsecond pulse. Therefore, since the 40 microsecond pulse is longer than the 6 microsecond pulse, it will dominate the operation of the flip-flop and turn it to a "0", even if the flip-flop was turned on by the 6 microsecond pulse from pin 4 of the other core. The reason for this operation is, that if both cores M602 and M603 have a "1" in them, both flip-flops will be turned off with the 40 microsecond output from the core; but, if either of the two cores (but not both) have a "1" in them, then one of the flip-flops will be turned on and since the other core would have a "0", it would have no output and one of the two flip-flops would be in the "1" condition. In normal operation this condition will alternate back and forth between cycles; i.e., one frame will be "even" and the next frame will be "odd". This condition will alternate back and forth between two flip-flops N622 and N623. The pin 8 outputs of these two flip-flops go to form the d-c level input to the two "AND" gates which were described in paragraph 3-2.7. as consisting of diodes CR602, resistors R608 and R607 or the "AND" gate consisting of CR605, resistors R611 and R612. In this operation, only one of these two "AND" gates will be open as described in paragraph 3-2.7, thus producing either an "even" set of pulses or an "odd" set of pulses. These will operate on the 10 Bit Shift Register as described in paragraph 3-3 so that the data may be shifted from the core to one of two independent outputs for the parallel data readout. This operation is also used in the four flip-flops N618 through N621.

3-2.11. During the ODD-EVEN comparison, the data which was in core M602 and in core M603 were bits #41 and #42. These two data bits have now been shifted to cores M603 and M604 with bit #43 being in core M602. The output of core M602 has two other outputs, one to an "AND" gate consisting of capacitor C632 with resistors R654 and R655, and the other to an "AND" gate consisting of capacitor C634 with resistor R657 and R658. The d-c level input to these two "AND" gates is either an "even gate" or an "odd gate" (figure 9-2). Therefore, the output of core M602 will be inserted into flip-flop N618 or N619, depending upon which gate is a "1". The "0" input to these flip-flops (pin 5) was reset just before by the "odd reset trigger" or the "even reset trigger" through capacitors C633 or C635, and, since only one of these inputs will be available at one time, only one of the flip-flops will be reset and new data would be inserted in the same flip-flop that was reset. At the end of the 50 microsecond "reset" pulse, the "or'ed" input of the positive going edge of the negative pulse, from either one-shot N604 or one-shot N606, would produce another input trigger to core driver N615 to produce one more core drive shift trigger pulse. This trigger pulse will drive the cores and insert new data in the flip-flops 50 microseconds after reset time.

This data will remain in the flip-flops until a new set of data has arrived from the Computer and is ready to be inserted again. The flip-flops have been reset to a "0" condition only for 50 microseconds before new data is read in. The "1" input of flip-flops N620 and N621 are from core M603 and core M604, respectively. The "odd gate" and "even gate" are "or'ed" together through diodes CR630 and CR631, thus opening both "AND" gates to pin 3 of flip-flops N620 and N621 at the same time. Both flip-flops were reset by either an "odd gate" or "even gate" through diodes CR632 and CR633 which reset both flip-flops N620 and N621 to the "0" condition and one or the other of the two flip-flops will get the new data depending on which frame ("odd" frame or "even" frame) that is received. On "odd" frames, flip-flop N621 would receive a "1"; on "even" frames, flip-flop N620 would receive a "1".

3-2.12. The protection circuit, consisting of flip-flops N622 and N623, should prevent both of these flip-flops from receiving a "1", as the data would be erroneous and would have no significance.

3-2.13. The auxiliary pin 7 output of flip-flop N621 triggers one-shot N626, producing a 20 millisecond pulse which is used to operate a high speed mercury relay. When this mercury relay is operated, it opens a set of contacts which are used for a "timing output" in which the contacts are open for approximately 20 milliseconds each time (flip-flop N621 receives a "1") there is an "odd" frame of data. Since the relay is controlled by one-shot operation, the one-shot will return to its quiescent condition and therefore the relay will de-energize and close the contacts so they are ready for the next cycle. This timing pulse will normally be received once every other frame of data or once per second.

3-2.14. Test Circuit - Networks N628 through N632 are used for the operation of a test circuit. This system may be tested without the need of any other associated equipment except possibly an oscilloscope.

3-2.14.1. The TEST START pushbutton S602 triggers 25 millisecond one-shot N628. The delayed pulse triggers 100 millisecond one-shot N629. In 100 milliseconds, N628 will be re-triggered by the delayed output of N629, thus producing and repeating pulse once every 125 milliseconds. The pin 7 output of one-shot N628 triggers flip-flop N630 to the "1" condition. The output of flip-flop N630 through zener diode CR646 produces a "test select and ready" pulse. Through the normal chain of events which was described in the operation of the chassis, the rise of "select and ready" will produce an "D/A-T/R ready" pulse. This pulse goes through switch S601D and will trigger one-shot N631 in test operation, producing a 10 microsecond "test sample" pulse. The output of one-shot N631 through zener diode CR647 produces the "test sample" pulses. The delayed output of this one-shot will trigger counting flip-flop N632, which will divide the incoming pulses on pin 7 by 2. This produces the necessary gating so that an alternate "1"s and "0"s pattern may be formed. When switch S601 is in position 3 or position 4, alternate "1"s and "0"s pattern is produced and is coupled from the pin 8 output of the counter through S601C through diode CR650 and produces the "test data" pulses. When in position 2 or in position 5, an all "0"s or all "1"s pattern is produced, which is either -20 volts for a "0" pattern and 0 volts for a "1" pattern. Zener diode CR650 adds a plus 10 volts to this pulse so that a +10 volt signal is available for the "1" input. Each time a "test sample" pulse was produced in the 260 microseconds (approximately), a "D/A-T/R ready" pulse was produced which produced the next "test sample" pulse through one-shot N631. This process is repeated until "select and ready" falls which is controlled by flip-flop N630. Flip-flop N630 is turned off by the counting signal when the "AND" gate consisting of resistors R693 and R694 is opened by one-shot N628. This causes "test select and ready" to drop, so that the indicator lights on the output of the Shift Registers should show the test pattern. The four patterns, which the TEST SELECTOR switch allows the operator to use, consist of all "0"s, all "1"s, "1-0", and "0-1". The Operation Chapter (Chapter 4) of this manual describes which lights should be lit for each position of the switch.

3-2.14.2. Switch S604, an EVEN-ODD-NORMAL switch, is used to fool the operation of flip-flops N622 and N623. When either in the "even" or the "odd" position, the switch will turn on both of the two flip-flops and hold them in that condition through the gating consisting of resistors R6108 and R6109 through diode CR634 to the "0" input for flip-flops N622 and N623. The pin 8 outputs are then switched to 0 volts in order to open one "AND" gate or the other. The two "AND" gates are connected to these outputs. The operation of this switch will only affect the circuit during TEST operation, as it receives its voltage through selector switch S601D terminal 14 (0 volts) and S601B, terminal 8 (+12 volts) which only receives a voltage during TEST operation. When in OPERATE, any position of this switch will have no effect upon the operation of the system.

3-2.15. Switch S605 VOLTAGE SELECTOR is used to select the voltage which the meter will monitor. The meter monitors the incoming a-c line voltages in the second position which is labeled ACØ. When in the second position, the a-c voltage is rectified by CR652 and applied through meter resistor R6103 to the meter. In the next position labeled +12V, the meter is reading the output voltage of the +12 volt Power Supply and in the 4th position, labeled -20V, it reads the output of the -20 volt Power Supply. In the last position labeled -85V, it reads the output of the -85 volt Power Supply. The operation of each of the positions is identical and meter resistors R6103 through R6107 are chosen so that the meter reading of 10 is read when the Power Supplies are in correct adjustment. Each minor division on the meter represents a 2% error on the output voltage of the Power Supplies.

3-2.16. Switch S603 (POWER) is used to turn ON and OFF the a-c power to the power contactor which is found in the lower portion of the rack mounted to the plug panel mounting bracket.

3-3. POWER CONTACTOR

The power contactor is found on the plug mounting bracket located at the lower rear of the rack. Its purpose is to switch the incoming a-c power. The controlling coil current is switched by the POWER switch located on the Control Chassis. When the switch is ON, the power contactor closes and applies a-c power to the two Power Supplies and to the Blower.

3-4. 10 BIT SHIFT REGISTER, MEC Model 76-8A (Figures 9-4, 9-5, and 9-6)

3-4.1. General - The function of the 10 Bit Shift Register is to receive two serial groups of 10 bits of data alternately. The groups are called "odd" and "even". The Register receives an "odd" or "even" group serially (M801 through M810) and shifts the group in parallel (depending on whether it is an "odd" or "even" group) to its respective set of flip-flops for independent output presentation. The odd set of flip-flops are N801, 3, 5, ...19, and the even set are N802, 4, 6, ...20. The data will remain in the flip-flops for accessibility until they are reset for acquisition of new data, and this time is approximately 100 microseconds, and not longer than 200 microseconds. The states of the flip-flops N801 through N820 are indicated by their respective neon indicators DS801 through DS820 on the front panel. When a flip flop is in a "1" state (a "1" state being the condition when pin 8 is at -17 volts), its associated indicator is on, and conversely when a flip-flop is in the "0" state (a "0" state being the condition when pin 8 is at 0 volts), its indicator is off. The indicators have been reversed bias at -2 volts by CR801 through CR803 and R865 to insure that the indicators will be off when the flip-flops are in the "0" state. C825, C826, and C827 are used as filter capacitors between the power voltages.

3-4.2. Detailed Description - The command pulses are developed in the Control Chassis. They are as follows: "Odd reset" and "even reset" triggers (from -20 volts to 0 volts, width 10 microseconds), "odd" flip-flop gate and "even" flip-flop gate (from -20 volts to 0 volts, width 200 microseconds), and core shift (from -20 volts to 0 volts, width 40 microseconds), 1000 cps. The "odd reset" trigger coming from the Control Chassis

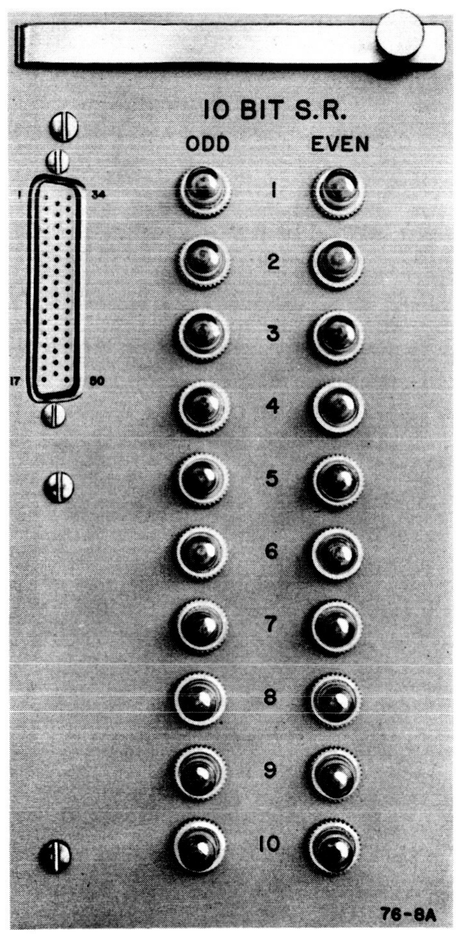


Figure 3-3. 10 Bit Shift Register

is capacity coupled through C829 to pin 3 of a one-shot N823. When pin 3 of N823 goes positive, then pin 7 of N823, the output, goes positive (from -20 volts to 0 volts, width 10 microseconds). This output ("odd reset") is capacity coupled through C824 to pin 5 of all the odd numbered flip-flops N801, 3, 5, ...19. Pin 5 of all the odd numbered flip-flops is biased in a quiescent condition at 7 volts by R851 and R862. Therefore, when pin 7 of N823 goes positive from (-20 volts to 0 volts 10 microseconds) pin 5 of all odd numbered flip-flops goes positive (from -7 volts to +10 volts, 10 microseconds) resetting the odd numbered flip-flops to the "0" state. At the same time that the "odd reset" trigger pulse enters the chassis, the "odd" flip-flop gate is received. The "odd" flip-flop gate is resistance coupled through R866 to pin 2 of N824 (TN58 consisting of two emitter followers). When pin 2 of the emitter follower N824 goes positive (from -20 volts to 0 volts, width 200 microseconds) and is directly coupled to R841 through R850 which is part of the " odd and" gates. There is an "odd" and "even and" gate associated with every magnetic core (M801 through M810), and these "and" gates are coupled to their respective flip-flops. The "odd" gate (output from pin 3 of the emitter follower) raises the voltage of pin 3 of all odd numbered flip-flops from -20 volts to -2 volts for 200 microseconds. This alone is not sufficient to trigger the flip-flops. The next shift pulse (from -20 volts to 0 volts, width 40 microseconds) will be 100 microseconds from the leading edge of the "odd" gate. Since the "odd" gate is 200 microseconds wide, this shift pulse will cause the read out from a core to be approximately in the middle of the gate (if there is a "1" present in the core). Assuming that there is a "1" in the core, a 10 microsecond pulse of 5 to 8 volts amplitude will be present at pin 4 of the cores. Pin 4 of the cores is capacity coupled through C801, 3, 5, ... 19 to "odd and" gates and through C802, 4, 6 ... 20 to "even and" gates. Therefore, the 5 to 8 volt pulses at pin 4 will be super-imposed on the "odd gate" and pin 3 of the odd numbered flip-flops will go positive enough (above 0 volts) to trigger the odd numbered flip-flops and a "1" state will be set. Both conditions have been satisfied at the "odd and" gates, therefore, only the odd numbered flip-flop will be triggered and the even numbered flip-flop will not be affected. The operation (a core string and core driver N821 with M811) is explained in detail in the Appendix. If there was a "0" in a core, when the shift pulse occurred, the odd numbered flip-flop will not change state because of the "odd and" gate and the 5 to 8 volt pulse from a core and the "odd" gate must be present at the same time in order for an odd numbered flip-flop to trigger. Therefore, at the time of the coincidence of the "odd" gate and shift pulse, all data in the cores is read out in parallel to the odd numbered flip-flop only. The next shift pulse occurs after the trailing edge of the "odd" gate and new data (1000 PPS) commences to be read in serially. Pin 8 of M801 is the data input. Pin 9 of M801 is directly coupled to pin 8 of M802 and pin 9 of M802 is directly coupled to pin 8 of M803. This is continued on to M810 and pin 9 of M810 is data output in the event another Shift Register is used. Many of these Shift Registers may be coupled together in a serial form to facilitate any number of bits in a word.

3-4.3. After the last bit of new data has been received by the cores, an "even reset" trigger (from -20 volts to 0 volts, width 10 microseconds) enters the chassis, and is capacity coupled through C828 to pin 3 of a one-shot N822. When pin 3 goes positive (from -20 volts to 0 volts, width 10 microseconds) the output pin 7 goes positive (from -20 volts to 0 volts, width 10 microseconds) and is capacity coupled through C823 to pin 5 of all the even numbered flip-flops (N802, 4, 6.... 20). Pin 5 is biased in a quiescent condition at -7 volts by R863 and R864. Therefore, when pin 7 of N822 goes positive (from -20 volts to 0 volts, width 10 microseconds) pin 5 of all the even numbered flip-flops goes positive (from -7 volts to above 0 volts, 10 microseconds) resetting the even numbered flip-flops to the "0" state. At the same time that the "even reset" trigger pulse enters the chassis, the even flip-flop gate is received. The even flip-flop gate is resistance coupled through R867 to pin 7 of an emitter follower (N824). When pin 7 goes positive (from -20 volts to 0 volts, width 200 microseconds), the output pin 5, (called even gate), goes positive (from -20 volts to 0 volts, width 200 microseconds) and is directly coupled to R851 through R860 which is part of the even "and" gates. The even "and" gates are coupled to pin 3 of the even flip-flops. Therefore when pin 6 of N824 goes positive, all pin 3's of the even flip-flops go positive (from -20 volts to -2 volts, width 200 microseconds). This will not trigger the flip-flops since a pulse equal to or greater than 0 volts is necessary. The "even and" gate requires an additional input in order to trigger the even flip-flops and this input will come from the cores if there is a "1" present in the cores. The first shift pulse that occurs after the "even" gate will be 100 microseconds from the leading edge of the "even" gate. Since the "even" gate is 200 microseconds wide, this shift pulse will cause the readout from a core to be approximately in the middle of the gate (if there is a "1" present in the core). Assuming that there was a "1" in the core, a 10 microsecond pulse, 5 to 8 volts will be present at pin 4 of the core. Pin 4 of the cores is capacity coupled to the Odd and Even "and" gates. Therefore, the output from the core (5 to 8 volt pulse) will be superimposed on the "even" gate and pin 3 of the even flip-flops will go positive enough (above 0 volts) to trigger the even flip-flops and a "1" state will be set. Both conditions have satisfied at the "even and" gate, and only the even flip-flops can be set. The odd flip-flops will not be affected by the output from the cores. If there was a "0" in a core when the shift pulse occurred, the even flip-flop will not change state because the "even and" gate and the 5 to 8 volt pulse from a core and the "even and" gate must be present at the same time in order for an even flip-flop to trigger. Therefore, at the time of coincidence of the Even Gate and shift pulse, all data in the cores is read out in parallel to the even flip-flops only. The next shift pulse occurs after the trailing edge of the "even gate", and new data commences to be read in. The next gate will be the "odd gate", occurring after the last bit of this new data has been received. This completes one cycle of operation, the length of a cycle being determined by the system.

CHAPTER IV
OPERATION

4-1. GENERAL

With all rack connectors properly connected and the a-c input power supplied to the Transfer Register, the following steps are required for operation.

4-2. POWER "ON"

a. Place the a-c power switch, located at the lower rear of rack, to the ON position. The red indicator lamp will glow. Place the POWER switch located on the Control Chassis to the ON position, the red indicator light on the Control Chassis will glow. This applies power to the Power Supplies and the Blower. CAUTION: if the Blower is not operating, check in the rear of the rack to make sure that the power switch located on the blower itself is in the high position. The BLOWER MUST OPERATE or the POWER switch must be turned OFF.

b. Check the voltage outputs of both the Power Supplies utilizing the meter located on the Control Chassis. Rotate the VOLTAGE SELECTOR switch to each position and observe the meter which is indicating the output voltage in that position. The meter should indicate a reading of 10 on each position, and the power supply voltages should be within this reading by ±5%. For a more accurate adjustment of each Power Supply, an accurate voltmeter may be used to adjust the operating voltages.

4-3. TEST

a. Rotate the TEST SELECTOR switch to PATTERN 1. Push the TEST START pushbutton. Switch the EVEN-ODD-NORMAL toggle switch (test pattern gating switch- S604) to the EVEN position. The neon indicators should remain off. Move the toggle switch to ODD. The neon indicator should still be off.

b. Rotate the TEST SELECTOR switch to PATTERN 2. Push the TEST START pushbutton. Switch the EVEN-ODD-NORMAL toggle switch to the EVEN position. The neon indicators numbers 1, 3, 5, 7, and 9 EVEN, on the 10 Bit Shift Register, should be lit. Move the EVEN-ODD-NORMAL toggle switch to the ODD position. The neon indicators 1, 3, 5, 7, and 9 ODD should be lit.

c. Rotate the TEST SELECTOR switch to PATTERN 3. Push the TEST START pushbutton. Switch the toggle switch to the EVEN position. The neon indicators numbers 2, 4, 6, 8, and 10 EVEN should be lit. Move the toggle switch to ODD. The neon indicators 2, 4, 6, 8, and 10 ODD should be lit.

d. Rotate the TEST SELECTOR switch to PATTERN 4. Push the TEST START pushbutton. Switch the toggle switch to the EVEN position. All neon indicators should be lit, in the EVEN row. Move the toggle switch to ODD, all ODD indicators should remain lit.

e. Switch the toggle switch to the NORMAL position. Rotate the TEST SELECTOR switch to PATTERN 3 and PATTERN 2. When moving the TEST SELECTOR switch between PATTERN 2 and PATTERN 3 it will be noted that, in one position, all of the

ODD frames will be alternate "1"s and "0"s and in the other position, the EVEN frames will be alternate "1"s and "0"s. This is the check which is given to the ODD-EVEN frame selection bits #41 and #42.

f. With the toggle switch in the NORMAL position, rotate the TEST SELECTOR switch to PATTERN 1 and PATTERN 4. The last input data should remain in the registers, because if bits #41 and #42 are both "1"s or both "0"s, the new data should be rejected and should not change from the previous input which was selected by either PATTERN 2 or PATTERN 3.

4-4. OPERATE

Rotate the TEST SELECTOR switch to OPERATE. The system is now ready for operation.

> NOTE: Before OPERATION, it is recommended that the operator read and understand the THEORY OF OPERATION section of this manual.

Lights #1 - #7 of SR #1 will always remain OFF, due to the modification of the core string.

CHAPTER V

INSTALLATION

5-1. GENERAL

No special considerations are necessary in selecting a site for the Transfer Register. This unit is completely self-contained and the rack provides adequate shielding for operation under normal operating environments.

5-2. INPUT AND OUTPUT CONNECTIONS

External connections to the Transfer Register are made through seven different MS type connectors. Tables 5-1 through 5-7 list each connector and its associated cable information.

5-3. INITIAL ADJUSTMENTS

There are no initial adjustments required prior to operation of the equipment. However, it is strongly urged that the Theory of Operation and the Operation chapters be read and understood before trying to operate the equipment.

TABLE 5-1.

AC POWER CONNECTOR J15

Terminal	Idendification	Wire
A	120 VAC Ø 1	#12
B		
C	120 VAC Common	#12

TABLE 5-2.

OUTPUT CONNECTOR TO D-A J16

Terminal	Identification	Wire
A		
B	Data to D/A	RG62/U
C		
D	Select and Ready to D/A	RG62/U
E		
F		
G		
H	D/A Ready (from the D/A)	RG62/U
J	Signal Ground	#18
K	Sample to D/ A	RG62/U
L		
M		
N		
P		
R		
S		
T		
U		
V		

TABLE 5-3.

DATA OUTPUT CONNECTOR J17

Terminal	Identification	Wire
1		
A		
2	Bit #43 Odd	*
B	Bit #44 Odd	*
3	Bit #45 Odd	*
C	Bit #46 Odd	*
4	Bit #47 Odd	*
D	Bit #48 Odd	*
5	Bit #49 Odd	*
E	Bit #50 Odd	*
6	Bit #51 Odd	*
F	Bit #52 Odd	*
7	Bit #53 Odd	*
G	Bit #54 Odd	*
8	Bit #55 Odd	*
H	Bit #56 Odd	*
9	Bit #57 Odd	*
I	Bit #58 Odd	*
10	Bit #59 Odd	*
J	Bit #60 Odd	*
11	Bit #61 Odd	*
K	Bit #62 Odd	*
12	Bit #63 Odd	*
L	Bit #64 Odd	*
13	Bit #65 Odd	*
M	Bit #66 Odd	*
14	Bit #67 Odd	*
N	Bit #68 Odd	*
15	Bit #69 Odd	*
0	Bit #70 Odd	*
16	Bit #71 Odd	*
P	Bit #72 Odd	*
17	Bit #73 Odd	*
Q	Bit #74 Odd	*
18	Bit #75 Odd	*
R	Bit #76 Odd	*
19	Bit #77 Odd	*
S	Bit #78 Odd	*
20	Bit #79 Odd	*
T	Bit #80 Odd	*
21	Bit #81 Odd	*
U	Bit #82 Odd	*
22	Bit #83 Odd	*
V	Odd Frame (Bit #41)	*
23		
W		
24		
X		
25		
Y		
+	Signal Ground	**
-	Signal Ground	**

TABLE 5-4.

DATA OUTPUT CONNECTOR J18

Terminal	Identification	Wire
1		
A		
2	Bit #43 Even	*
B	Bit #44 Even	*
3	Bit #45 Even	*
C	Bit #46 Even	*
4	Bit #47 Even	*
D	Bit #48 Even	*
5	Bit #49 Even	*
E	Bit #50 Even	*
6	Bit #51 Even	*
F	Bit #52 Even	*
7	Bit #53 Even	*
G	Bit #54 Even	*
8	Bit #55 Even	*
H	Bit #56 Even	*
9	Bit #57 Even	*
I	Bit #58 Even	*
10	Bit #59 Even	*
J	Bit #60 Even	*
11	Bit #61 Even	*
K	Bit #62 Even	*
12	Bit #63 Even	*
L	Bit #64 Even	*
13	Bit #65 Even	*
M	Bit #66 Even	*
14	Bit #67 Even	*
N	Bit #68 Even	*
15	Bit #69 Even	*
0	Bit #70 Even	*
16	Bit #71 Even	*
P	Bit #72 Even	*
17	Bit #73 Even	*
Q	Bit #74 Even	*
18	Bit #75 Even	*
R	Bit #76 Even	*
19	Bit #77 Even	*
S	Bit #78 Even	*
20	Bit #79 Even	*
T	Bit #80 Even	*
21	Bit #81 Even	*
U	Bit #82 Even	*
22	Bit #83 Even	*
V	Even Frame (Bit #42)	*
23		
W		
24		
X		
25		
Y		
+	Signal Ground	**
-	Signal Ground	**

* #22 Shield Wire, Low Capacity

** Shields of above cable

TABLE 5-5.

DATA OUTPUT CONNECTOR J19

Terminal	Identification	Wire
1	Bit #84 Odd	*
A	Bit #84 Even	*
2	Bit #85 Odd	*
B	Bit #85 Even	*
3	Bit #86 Odd	*
C	Bit #86 Even	*
4	Bit #87 Odd	*
D	Bit #87 Even	*
5	Bit #88 Odd	*
E	Bit #88 Even	*
6	Bit #89 Odd	*
F	Bit #89 Even	*
7	Bit #90 Odd	*
G	Bit #90 Even	*
8	Bit #91 Odd	*
H	Bit #91 Even	*
9	Bit #92 Odd	*
I	Bit #92 Even	*
10	Bit #93 Odd	*
J	Bit #93 Even	*
11	Bit #94 Odd	*
K	Bit #94 Even	*
12	Bit #95 Odd	*
L	Bit #95 Even	*
13	Bit #96 Odd	*
M	Bit #96 Even	*
14	Bit #97 Odd	*
N	Bit #97 Even	*
15	Bit #98 Odd	*
O	Bit #98 Even	*
16	Bit #99 Odd	*
P	Bit #99 Even	*
17	Bit #100 Odd	*
Q	Bit #100 Even	*
18	Bit #101 Odd	*
R	Bit #101 Even	*
19	Bit #102 Odd	*
S	Bit #102 Even	*
20	Bit #103 Odd	*
T	Bit #103 Even	*
21		
U		
22		
V		
23		
W		
24		
X		
25		
Y		
+	Signal Ground	**
-	Signal Ground	**

TABLE 5-6.

INPUT CONNECTOR FROM COMPUTER J20

Terminal	Identification	Wire
A		
B	Data from Computer	RG62/U
C		
D	Select and Ready from Computer	RG62/U
E		
F	D/A-T/R Ready to Computer	RG62/U
G	Signal Ground	#18
H	Sample from Computer	#18

TABLE 5-7.

OUTPUT CONNECTOR J21

Terminal	Identification	Wire
A	Signal Ground	#18
B	Timing } Contact Closure (Contacts are Normally Closed)	#22
C	Timing } Contact Closure (Contacts are Normally Closed)	#22
D		

* #22 Shielded Wire, low capacity
** Shields of above cable

CHAPTER VI

MAINTENANCE

6-1. GENERAL

Since all of the circuitry within the Transfer Register is made up entirely of semi-conductor circuits and magnetic cores, it is not expected that malfunction will occur for long periods of operation. However, malfunction of individual parts is expected and can be located by normal trouble shooting operation. The only necessary test equipment for normal maintenance of the Transfer Register is an oscilloscope and an accurate VOM meter. Many of the malfunctions can be located by observing the neon lamps located on the front panel of the various chassis.

6-2. PREVENTIVE MAINTENANCE

Preventive maintenance is recommended for the following parts of equipment.

a. The Blower filter should be removed and cleaned in a solution of warm water and detergent or cleaned with a vacuum cleaner at least once each week.

b. The adjustments of the voltage control on each of the Power Supplies should be checked at the beginning of each operation to see if the correct voltage may need adjusting by this control.

6-3. ELECTRO-MECHANICAL DEVICES

If any of the relays do not function properly, the complete sub-assembly should be replaced and the malfunctioning unit returned to the manufacturer for possible repairs.

CHAPTER VII

PARTS LIST

The MEC Model 79 Transfer Register consists of the following assemblies:

Quantity	Assembly	Page
1	MEC Model 79-6A Control Chassis	7-3
6	MEC Model 76-8A 10 Bit Shift Register	7-7
1	MEC Model 79-1AAA Connector Bracket	7-8
1	MEC Model 165-4C Power Supply	7-9
1	MEC Model 76-9A Power Supply	7-12
1	Blower	7-13

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
6-1				MEC 79-6A	ASSEMBLY, CONTROL	1	
6-2	C601			Cornell Dubilier PM6S6	CAPACITOR, Fixed Mylar, .06μf 600 vdc	1	
6-3	C602			Cornell Dubilier PM4P1	CAPACITOR, Fixed Mylar, .1μf 400 vdc	1	
6-4	C603 C607 C637			MIL CM-19B-152K	CAPACITOR, Fixed Mica, 1500$\mu\mu$f 500 vdc ±10%	3	
6-5	C604 C608			Cornell Dubilier PM6D5	CAPACITOR, Fixed Mylar, .005μf 600 vdc	2	
6-6	C605 C609 C622 C626 C633 C635 C646			MIL CM-19B-681K	CAPACITOR, Fixed Mica, 680μf 500 vdc ±10%	7	
6-7	C606 C610			Cornell Dubilier PM4S1	CAPACITOR, Fixed Mylar, .01μf 400 vdc	2	
6-8	C611, C639 C615, C640 C617, C642 C618, C643 C619, C647 C620 C623-C625 C628-C630 C663 C664, C653 C655, C659			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000$\mu\mu$f 500 vdc±10%	22	
6-9	C645			Cornell Dubilier PM4S5	CAPACITOR, Fixed Mylar, .05μf, 400 vdc	1	
6-10	C613			MIL CM-19B-471K	CAPACITOR, Fixed Mica, 470$\mu\mu$f, 500 vdc, ±10%	1	
6-11	C614			MIL CM-19B-331K	CAPACITOR, Fixed Mica, 330$\mu\mu$f, 500 vdc, ±10%	1	
6-12	C616			MIL CM-42E-183J	CAPACITOR, Fixed Mica, 18,000$\mu\mu$f, 500 vdc, ±5%	1	
6-13	C621, C648, C652, C654, C657, C660, C662			Fansteel F110-1	CAPACITOR, (Blu-Cap), 10μf, 25 vdc	7	
6-14	C627			Cornell Dubilier PM6D68	CAPACITOR, Fixed Mylar, .0068μf, 600 vdc	1	
6-15	C631 C658			MIL CM-19B-202K	CAPACITOR, Fixed Mica, 2000$\mu\mu$f, 500 vdc, ±10%	2	
6-16	C632, C634 C636, C638			MIL CM-19B-222K	CAPACITOR, Fixed Mica, 2200$\mu\mu$f, 500 vdc, ±10%	4	
6-17	C641			MIL CM-35B-123K	CAPACITOR, Fixed Mica, 12,000$\mu\mu$f, 500 vdc, ±10%	1	
6-18	C644			Fansteel F120-1	CAPACITOR, (Blu-Cap), 2μf, 100 vdc	1	
6-19	C649, C651 C656			MIL CM-19B-561K	CAPACITOR, Fixed Mica, 560$\mu\mu$f, 500 vdc, ±10%	3	
6-20	C650			G. E. 29F712	CAPACITOR, Tantalytic, 2.5μf, 10 vdc	1	
6-21	C661			Fansteel F308-1	CAPACITOR, (Blu-Cap), 100μf, 30 vdc	1	
6-21A	C612			Cornell Dubilier	CAPACITOR, Fixed Mylar, .015μf, 400 vdc	1	
6-21B	C666			Elmenco IDP-2-753	CAPACITOR, Mylar Paper, .075μf, 100 vdc	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
6-22	CR601-CR607 CR611-CR620 CR622-CR625 CR627 CR630 CR634 CR636 CR640-CR645 CR648 CR649 CR650 CR654-CR656			Transitron T12G or Clevite CTP-503	DIODE	40	
6-23	CR608			International Rectifier IN1521	DIODE, Zener (1Z6.8)	1	
6-24	CR609 CR626 CR628 CR629 CR653			Pacific Semi-Conductor IN703	DIODE, Zener	5	
6-25	CR610 CR637 CR638 CR639			G. E. IN1692	DIODE	4	
6-26	CR621			International Rectifier IN1524	DIODE, Zener (1Z12)	1	
6-27	CR635			International Rectifier IN1518	DIODE, Zener (1Z3.9)	1	
6-28	CR646 CR747 CR650			International Rectifier IN1523	DIODE, Zener (1Z10) 10V	3	
6-29	CR652			G. E. IN1695	DIODE	1	
6-30	DS601 DS602			MEC 16-102	INDICATOR	2	
6-31	DS603			Eldema 1CG12-4535	LAMP, Neon to Spec. 21C-3864-7	1	
6-32	I601			Dialight Corp. S6	LAMP, Incandescent, Bayonet Type, 6W 24V	1	
6-33	F601			Bussmann AGC	FUSE, 3 Amp	1	
6-34	K601			MEC RY-12	RELAY, Mercury wetted	1	
6-35	M601			MEC MN-13	CORE, Magnetic	1	
6-36	M602-M604			MEC MN-11	CORE, Magnetic	3	
6-37	MV601			Beede E-25	METER, 1.2 MA (Scale 0-12) Horizontal Mounting	1	
6-38	N601, N608 N612			MEC TN-57	TRANSISTOR NETWORK	3	
6-39	N602-N607 N609, N613 Cont'd.			MEC TN-138B	TRANSISTOR NETWORK	16	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
6-39 Cont'd.	N614, N617 N624, N626-N629, N631						
6-40	N610, N630			MEC TN-90B	TRANSISTOR NETWORK	2	
6-41	N611			MEC TN-58	TRANSISTOR NETWORK	1	
6-42	N615			MEC TN-130B	TRANSISTOR NETWORK	1	
6-43	N616, N622 N623			MEC TN-28	TRANSISTOR NETWORK	3	
6-44	N618, N619 N620, N621			MEC TN-144	TRANSISTOR NETWORK	4	
6-45	N625			MEC TN-154	TRANSISTOR NETWORK	1	
6-46	N632			MEC TN-42	TRANSISTOR NETWORK	1	
6-47	M633			MEC TN-158	TRANSISTOR NETWORK	1	
6-48	P601			Cannon DD-50P	PLUG	1	
6-49	R601, R618 R640			MIL RC42GF910J	RESISTOR, Fixed composition, 91Ω ±5% 2W	3	
6-50	R602, R603 R619, R622 R625, R641 R642, R644 R649, R672 Cont'd.			MIL RC20GF103K	RESISTOR, Fixed composition, 10K ±10% 1/2W	17	
6-50 Cont'd.	R674, R680 R685, R695-R697, R6101						
6-51	R604, R606 R609, R613 R628, R631 R643, R646 R663, R667 R670, R671 R673, R675 R681, R682 R688, R691			MIL RC20GF473K	RESISTOR, Fixed composition, 47K ±10% 1/2W	18	
6-52	R605, R632 R652, R689			MIL RC20GF153K	RESISTOR, Fixed composition, 15K ±10% 1/2W	4	
6-53	R607, R611 R626, R629 R693			MIL RC20GF333K	RESISTOR, Fixed composition, 33K ±10% 1/2W	5	
6-54	R608, R612 R616, R656 R659, R662 R694, R699			MIL RC20GF332K	RESISTOR, Fixed composition, 3300Ω ±10% 1/2W	8	
6-55	R610, R614 R648			MIL RC20GF223K	RESISTOR, Fixed composition, 22K ±10% 1/2W	3	
6-56	R615, R651 R666, R669			MIL RC20GF152K	RESISTOR, Fixed composition, 1500Ω ±10% 1/2W	4	
6-57	R617, R676			MIL RC20GF471K	RESISTOR, Fixed composition, 470Ω ±10% 1/2W	2	
6-58	R621, R633 R635, R636 R645, R647 R679, R6100 R6110			MIL RC20GF222K	RESISTOR, Fixed composition, 2200Ω ±10% 1/2W	9	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
6-59	R623			MIL RC20GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1/2W	1	
6-60	R624			MIL RC20GF682K	RESISTOR, Fixed composition, 6800Ω ±10% 1/2W	1	
6-61	R627, R630 R634, R668 R690, R698 R6108			MIL RC20GF472K	RESISTOR, Fixed composition, 4700Ω ±10% 1/2W	7	
6-62	R637 R639			MIL RC20GF271K	RESISTOR, Fixed composition, 270Ω ±10% 1/2W	2	
6-63	R638			MIL RC20GF101K	RESISTOR, Fixed composition, 100Ω ±10% 1/2W	1	
6-64	R650			MIL RC20GF203J	RESISTOR, Fixed composition, 20K ±5% 1/2W	1	
6-65	R653, R683 R686, R687			MIL RC20GF102K	RESISTOR, Fixed composition, 1K ±10% 1/2W	4	
6-66	R654, R657 R660, R664 R6102, R6111-R6113			MIL RC20GF104K	RESISTOR, Fixed composition, 100K ±10% 1/2W	8	
6-67	R655, R658 R661, R665			MIL RC20GF113J	RESISTOR, Fixed composition, 11K ±5% 1/2W	4	
6-68	R677			MIL RC20GF112J	RESISTOR, Fixed composition, 1100Ω ±5% 1/2W	1	
6-69	R678 R6109			MIL RC20GF823K	RESISTOR, Fixed composition, 82K ±10% 1/2W	2	
6-70	R684			MIL RC20GF183K	RESISTOR, Fixed composition, 18K ±10% 1/2W	1	
6-71	R6103			Phaostron CA4RS-1/2	RESISTOR, Precision, 51.4K ±1% 1/2W	1	
6-72	R6104			Pnaostron CA4RS-1/2	RESISTOR, Precision, 12K ±1% 1/2W	1	
6-73	R6105			Phoastron CA4RS-1/2	RESISTOR, Precision, 17K ±1% 1/2W	1	
6-74	R6106			Phaostron CA4RS-1/2	RESISTOR, Precision, 20K ±1% 1/2W	1	
6-75	R6107			Phaostron CA4RS-1/2	RESISTOR, Precision, 85K ±1% 1/2W	1	
6-76	R620			MIL RC20GF273K	RESISTOR, Fixed composition, 27K ±10% 1/2W	1	
6-77	S601			Centralab PA-2027	SWITCH, Rotary	1	
6-78	S602			Micro 2PB11	SWITCH, Pushbutton	1	
6-79	S603			Carling 2GL63-73	SWITCH, Toggle, DPDT	1	
6-80	S604			Carling 2GM63-73	SWITCH, Toggle, DPDT	1	
6-81	S605			Centralab PA-2005	SWITCH, Rotary	1	
6-82	TJ601			Cannon DD-50S	Connector	1	
6-83	XDS603			Eldema 11H4593	INDICATOR HOLDER	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
6-84	XF601			Bussmann HKP	FUSE HOLDER	1	
6-85	XI601			Dialight Corp. 103-3502-1211	INDICATOR HOLDER, Dome Type, Clear Red Lens, For S6 Bayonet Type Lamp	1	
6-86	XM601-XM604			JAN TS103P02	SOCKET, 9 Pin Miniature, Mica filled	4	
6-87	XN601-XN633 XK601			JAN TS101P01	SOCKET, Octal, Mica filled	34	
6-88				Whitso K-105	KNOB	2	
6-89				Eldema 11H-4119	LENS CAP (red)	1	
8-1				MEC 76-8A	ASSEMBLY, 10-BIT SHIFT REGISTER	1	
8-2	C801-C822			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000$\mu\mu$f ±10% 500 vdc	22	
8-3	C823 C824			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01μf 400 vdc	2	
8-4	C825			Fansteel F110-1	CAPACITOR, (Blu-Cap) 10μf 25 vdc Insulated Case.	1	
8-5	C826 C827			Fansteel F308-1	CAPACITOR, (Blu-Cap) 100μf 30 vdc	2	
8-6	C828 C829			MIL CM-19B-331K	CAPACITOR, Fixed, Mica, 330$\mu\mu$f ±10% 500 vdc	2	
8-7	CR801-CR803			G. E. IN1692	DIODE	3	
8-8	CR804			Clevite CTP-503	DIODE	1	
8-9	DS801-DS820			MEC 16-102	INDICATOR	20	
8-10	M801-M810			MEC MN-11	CORE, Magnetic	10	
8-11	M811			MEC MN-13	CORE, Magnetic	1	
8-12	N801-N820			MEC TN-144	TRANSISTOR NETWORK	20	
8-13	N821			MEC TN-130B	TRANSISTOR NETWORK	1	
8-14	N822 M823			MEC TN-138B	TRANSISTOR NETWORK	2	

1 ITEM NO.	2 REFER DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG AND PART NO	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
8-15	N824			MEC TN-58	TRANSISTOR NETWORK	1	
8-16	P801			Cannon DD-50P	PLUG	1	
8-17	R801			MIL RC20GF273K	RESISTOR, Fixed composition, 27K ±10% 1/2W	20	
8-18	R861-R864			MIL RC20GF103K	RESISTOR, Fixed composition, 10K ±10% 1/2W	4	
8-19	R841-R860			MIL RC20GF113J	RESISTOR, Fixed composition, 11K ±5% 1/2W	20	
8-20	R865			MIL RC20GF182K	RESISTOR, Fixed composition, 1800Ω ±10% 1/2W	1	
8-21	R866 R867			MIL RC20GF102K	RESISTOR, Fixed composition, 1K ±10% 1/2W	2	
8-22	R868			MIL RC20GF332K	RESISTOR, Fixed composition, 3.3K ±10% 1/2W	1	
8-23	R869			MIL RC20GF163J	RESISTOR, Fixed composition, 16K ±5% 1/2W	1	
8-24	TJ801			Cannon DD-50S	CONNECTOR	1	
8-25	R821-R840			MIL RC20GF104K	RESISTOR, Fixed composition, 100K ±10% 1/2W	20	
8-26	XM801-XM811			JAN TS103P02	SOCKET, 9 Pin Miniature, Mica filled	11	
8-27	XN801-XN824			JAN TS101P01	SOCKET, Octal, Mica filled	24	
1-1				MEC 79-1AAA	Assembly, Connector Bracket	1	
1-2	F1			Bussmann BAN	Fuse, 20 Amp	1	
1-3	I1			Dialight Corp. 6S6	Lamp, Incandescent, Candelabra Base 125V Clear	1	
1-4	J15			Cannon MS3102A-18-10P	Plug	1	
				Cannon MS3106B-18-10S	Connector	1	
				Cannon 3057-10	Cable Clamp	1	
1-5	J17 J19			Amphenol 97-3102A-36-404P	Plug	3	
				Amphenol 97-3106B-36-404S	Connector	3	
				Amphenol 3057-20	Cable Clamp	3	
1-6	J20			Cannon MS3102A-22-18P	Plug	1	
				Cannon MS3106B-22-18S	Connector	1	
				Cannon 3057-12	Cable Clamp	1	
1-7	J21			Cannon MS3102A-18-13P	Plug	1	
				Cannon MS3106B-18-13S	Connector	1	
				Cannon 3057-10	Cable Clamp	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
1-8	K1			Allen Bradley 702A0D92	Contactor	1	
1-9	S1			Cutler Hammer ST52N	Switch, Toggle, DPDT, 25 Amp, 125V (with Bright Nickel Handle)	1	
1-10	TB1			Cinch-Jones 2-140	Terminal Strip	1	
1-11	XF1			Bussmann HPC	Fuse Holder	1	
1-12	XI1			Dialight Corp 514001-111	Indicator Holder	1	
4-1				MEC 165-4C	ASSEMBLY, POWER SUPPLY	1	
4-2	C401 C402 C421-C423			Mallory 20-71937	CAPACITOR, Computer Grade, 4000μf 60 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	5	
4-3	C403 C425 C443 C444			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01μf 400 vdc	4	
4-4	C424			Cornell Dubilier PM4P1	CAPACITOR, Fixed, Mylar, .1μf 400 vdc	1	
4-5	C404 C426			Fansteel F308-1	CAPACITOR, Blu-cap, 100μf 30 vdc	2	
4-6	C441 C442			Mallory 20-71855	CAPACITOR, Computer Grade, 2000μf 100 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	2	
4-7	C445			Fansteel F316-1	CAPACITOR, Blu-cap, 30μf 100 vdc	1	
4-8	CR401 CR421			G. E. 4JA211AB1AC2	RECTIFIER	3	
4-9	CR402 CR422			International Rectifier IN1519	DIODE, Zener (1Z4.7)	2	
4-10	CR442			International Rectifier IN1524	DIODE, Zener (1Z12)	1	
4-11	F401 F403			Bussmann AGC	FUSE 1 Amp	2	
4-12	F402			Bussmann AGC	FUSE, 3 Amp	1	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
4-13	F404			Bussmann MDX	FUSE, Fusetron, Slo-Blow, 3 Amp.	1	
4-14	P401			Cannon DD-50P	PLUG	1	
4-15	Q423 Q442			Delco 2N553	TRANSISTOR, (Mount with Parts #100 & #101)	2	
4-16	Q401 Q421 Q441 Q422			Delco 2N443	TRANSISTOR, (Lug type Leads)	4	
4-17	Q402 Q403 Q424 Q443			G. E. 2N525	TRANSISTOR	4	
4-18	Q404 Q425 Q444			Sylvania 2N377A	TRANSISTOR	3	
4-19	R401, R402 R421A R421B R441 R442			Ward Leonard 5X1	RESISTOR, Axiohm, 1Ω 5W	6	
4-20	R403 R443			Ward Leonard 5X2	RESISTOR, Axiohm, 2Ω 5W	2	
4-21	R404 R425 R444			MIL RC42GF102K	RESISTOR, Fixed composition, 1K ±10% 2W	3	
4-22	R405			MIL RC42GF151K	RESISTOR, Fixed composition, 150Ω ±10% 2W	1	
4-23	R406			MIL RC20GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1/2W	1	
4-24	R407 R428 R447			MIL RC20GF101K	RESISTOR, Fixed composition, 100Ω ±10% 1/2W	3	
4-25	R408			MIL RC20GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1/2W	1	
4-26	R409 R430 R449			MIL RC20GF822K	RESISTOR, Fixed composition, 8.2K ±10% 1/2W	3	
4-27	R410 R431 R450			MIL RC20GF621J	RESISTOR, Fixed composition, 620Ω ±5% 1/2W	3	
4-28	R411 R432			MIL RC20GF472K	RESISTOR, Fixed composition, 4.7K ±10% 1/2W	2	
4-29	R412			MIL RC32GF121K	RESISTOR, Fixed composition, 120Ω ±10% 1W	1	
4-30	R414 R435			Chicago Tel. RA20LASB250A	POTENTIOMETER, 25Ω 2W	2	
4-31	R415			MIL RC32GF820J	RESISTOR, Fixed composition, 82Ω ±5% 1W	1	
4-32	R413			MIL RC42GF131J	RESISTOR, Fixed composition, 130Ω ±5% 2W	1	
4-33	R422			Ward Leonard 10F1	RESISTOR, Fixed, Wire wound, 1Ω 10W	1	
4-34	R423 R424			Ward Leonard 10F2	RESISTOR, Fixed, Wire wound, 2Ω 10W	2	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
4-35	R426 R437			Ward Leonard 10F150	RESISTOR, Fixed, Wire wound, 150Ω 10W	2	
4-36	R427 R446			MIL RC32GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1W	2	
4-37	R429 R448			MIL RC32GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1W	2	
4-38	R433 R416			MIL RC42GF271K	RESISTOR, Fixed composition, 270Ω ±10% 2W	2	
4-39	R436			MIL RC32GF510J	RESISTOR, Fixed composition, 51Ω ±5% 1W	1	
4-40	R434			MIL RC42GF181J	RESISTOR, Fixed composition, 180Ω ±5% 2W	1	
4-41	R451			MIL RC42GF302J	RESISTOR, Fixed composition, 3K ±5% 2W	1	
4-42	R453			Allen Bradley JLU-1011 or JA1L040S101UC	POTENTIOMETER, 100Ω 2W, Linear Taper	1	
4-43	R454			MIL RC42GF272J	RESISTOR, Fixed composition, 2.7K ±5% 2W	1	
4-44	R455			Ward Leonard 5X500	RESISTOR, Fixed, Axiohm, 500Ω 5W	1	
4-45	R452			MIL RC32GF561J	RESISTOR, Fixed composition, 560Ω ±5% 1W	1	
4-46	R445			Ward Leonard 10F250	RESISTOR, Fixed, Wire wound, 250Ω 10W	1	
4-47	T401			TTI 5486	TRANSFORMER	1	
4-48	TJ401- TJ404			H.H. Smith 221	JACK, Midget Banana (Black)	4	
4-49	XF401- XF404			Bussmann HKP	FUSEHOLDER	4	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE
9-1				MEC 76-9A	ASSEMBLY, POWER SUPPLY (-17V and -20V)	1	
9-2	C901-C905 C906			Mallory 20-71937	CAPACITOR, Computer Grade, 4000μf 60 vdc 2-1/16 x 4-1/4, Alum. can with Acetate Sleeve.	6	
9-3	C907			Cornell Dubilier PM4P5	CAPACITOR, Fixed, Mylar, .5μf 400 vdc	1	
9-4	C908			Mallory 20-71844	CAPACITOR, Computer Grade, 15,000μf 15 vdc 2-9/16 x 4-1/4 Alum. can with Acetate Sleeve	1	
9-5	CR901 CR902			G. E. ZJ50B(C60)	DIODE, 100 V	2	
9-6	CR903			Westinghouse IN1200	DIODE,	1	
9-7	CR904-CR907 CR909-CR911			G. E. IN1692	DIODE	7	
9-8	CR908			G. E. 4JA211BB1AC1	RECTIFIER	1	
9-9	L901			Sterling Trans. T3891	CHOKE	1	
9-10	N901			MEC TN-160	TRANSISTOR NETWORK	1	
9-11	Q901			Delco 2N443	TRANSISTOR, (Lug type Leads)	1	
9-12	R901			MIL RC20GF622J	RESISTOR, Fixed composition, 6.2K ±5% 1/2W	1	
9-13	R902			Ohmite CLU-1521 or JA1L040S152UC	POTENTIOMETER, 1.5K 2W, Linear Taper	1	
9-14	R903			MIL RC20GF621J	RESISTOR, Fixed composition, 620Ω ±5% 1/2W	1	
9-15	R904			MIL RC20GF331K	RESISTOR, Fixed composition, 330Ω ±10% 1/2W	1	
9-16	R905			Ohmite 0600A	RESISTOR, Fixed, Wire wound, 5Ω 100W (with Mounting Bracket #12)	1	
9-17	R906			MIL RC42GF332K	RESISTOR, Fixed composition, 3.3K ±10% 2W	1	
9-18	R907-R909			Ward Leonard 20F1	RESISTOR, Fixed, Wire wound, 1Ω 20W	3	
9-19	R910			MIL RC20GF101K	RESISTOR, Fixed composition, 100Ω ±10% 1/2W	1	
9-20	T901			Industrial Trans. MP-8610	TRANSFORMER	1	
9-21	T902			Sterling Trans. T-3890	TRANSFORMER	1	
9-22	T903			Chicago Trans. FMS-6	TRANSFORMER	1	
9-23	TJ901-TJ903			H.H. Smith 221	JACK, Midget Banana (Black)	3	
9-24	XN901			Amphenol 77-MIP-11T	SOCKET, 11 Pin	1	

1	2	3		4	5	6	7
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
1				McLean 2EB508C	ASSEMBLY, BLOWER	1	

CHAPTER VIII

WIRE LIST

INDEX

WIRE NO.	REFERENCE	SHEET NO.	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	J1	3		Shift Register #1		
	J2	6		Shift Register #2		
	J3	9		Shift Register #3		
	J4	12		Shift Register #4		
	J5	15		Shift Register #5		
	J6	18		Shift Register #6		
	J9	21		Control Chassis		
	J11	24		CC Supply (165-4C)		
	J14 OV BUS	27		76-9A Supply		
	J14 -17V BUS	28		76-9A Supply		
	J14 -20V BUS	29		76-9A Supply		
	J15	30		AC Input Connector		
	J16	31		D/A Output Connector		
	J17	32		Register Output Con- nector		
	J18	34		Register Output Con- nector		
	J19	36		Register Output Con- nector		
	J20	38		Input Connector		
	J21	39		Timing Output Connector		
	+12V BUS	40		165-4C Supply		
	OV BUS	41		165-4C Supply		
	-85V BUS	42		165-4C Supply		
	K1	43		AC Contactor		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 1 OF 50 SHEETS

INDEX

WIRE NO.	REFERENCE	SHEET NO.	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	TB1	44		Blower Term. Bd.		
	BL	45		Blower		
	I1	46		Indicator		
	F1 & F2	47		$\emptyset_1$ Fuse		
	S1	48		Main AC Switch		
	TB2	49		AC Neutral Bus		
	T903	50		76-9A Power Supply		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 2 OF SHEETS

J1

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J19-20	1	Bit#103 Odd, F/F #1	22	BK
	2	J19-T		Bit#103 Even, F/F #2	22	W/BK
	3	J19-19		Bit#102 Odd, F/F #3	22	BR
	4	J19-S		Bit#102 Even, F/F #4	22	W/BR
	5	J19-18		Bit#101 Odd, F/F #5	22	R
	6	J19-R		Bit#101 Even, F/F #6	22	W/R
	7	J19-17		Bit #100 Odd, F/F #7	22	O
	8	J19-Q		Bit #100 Even, F/F #8	22	W/O
	9	J19-16		Bit#99 Odd, F/F #9	22	Y
	10	J19-P		Bit#99 Even, F/F #10	22	W/Y
	11	J19-15		Bit#98 Odd, F/F #11	22	G
	12	J19-0		Bit#98 Even, F/F #12	22	W/G
	13	J19-14		Bit#97 Odd, F/F #13	22	BL
	14	J19-N		Bit#97 Even, F/F #14	22	W/BL
	15	J19-13		Bit#96 Odd, F/F #15	22	V
	16	J19-M		Bit#96 Even, F/F #16	22	W/V
	17	J19-12		Bit#95 Odd, F/F #17	22	S
	18	J19-L		Bit#95 Even, F/F #18	22	W/S
	19	J19-11		Bit#94 Odd, F/F #19	22	W
	20	J19-K		Bit#94 Even, F/F #20	22	BR/W
	21	J2-34		Core Driver Trigger	22	Y
	21	J1-34	1	Core Driver Trigger	22	Y

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 3 OF SHEETS

J1

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	22	J2-35	1	Odd Reset Trigger	22	O
	22	J1-35	1	Odd Reset Trigger	22	O
	23	J2-36	1	Even Reset Trigger	22	W/O
	23	J1-36	1	Even Reset Trigger	22	W/O
	24	J2-37	1	Odd FF Gate	22	G
	24	J1-37	1	Odd FF Gate	22	G
	25	J2-38	1	Even FF Gate	22	W/G
	25	J1-38	1	Even FF Gate	22	W/G
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J5-21	1	Core Driver Trigger	22	Y
	34	J1-21	1	Core Driver Trigger	22	Y
	35	J5-22	1	Odd Reset Trigger	22	O
	35	J1-22	1	Odd Reset Trigger	22	O
	36	J5-23	1	Even Reset Trigger	22	W/O
	36	J1-23	1	Even Reset Trigger	22	W/O
	37	J5-24	1	Odd F/F Gate	22	G
	37	J1-24	1	Odd F/F Gate	22	G
	38	J5-25	1	Even F/F Gate	22	W/G
	38	J1-25	1	Even F/F Gate	22	W/G

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 4 OF SHEETS

J1

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	39					
	40	J2-41	1	Core Output	22	BR
	41	J9 -34	1	*Core Input*	22	W/BR
	42	J14-17V-3	2	-17V	20	W/S
	43	J14-17V-3	2	-17V	20	W/S
	44	+12V-3	2	+12V	20	R
	45	J14-OV-3	2	OV	20	BK
	46	J14-OV-3	2	OV	20	BK
	47	J14-20V-3	2	-20V	20	S
	48	J14-20V-3	2	-20V	20	S
	49	-85V-3	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 5 OF SHEETS

J2

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J19-10	1	Bit #93 Odd, F/F #1	22	BK
	2	J19-J		Bit #93 Even, F/F #2	22	W/BK
	3	J19-9		Bit #92 Odd, F/F #3	22	BR
	4	J19-I		Bit #92 Even, F/F #4	22	W/BR
	5	J19-8		Bit #91 Odd, F/F #5	22	R
	6	J19-H		Bit #91 Even, F/F #6	22	W/R
	7	J19-7		Bit #90 Odd, F/F #7	22	O
	8	J19-G		Bit #90 Even, F/F #8	22	W/O
	9	J19-6		Bit #89 Odd, F/F #9	22	Y
	10	J19-F		Bit #89 Even, F/F #10	22	W/Y
	11	J19-5		Bit #88 Odd, F/F #11	22	G
	12	J19-E		Bit #88 Even, F/F #12	22	W/G
	13	J19-4		Bit #87 Odd, F/F #13	22	BL
	14	J19-D		Bit #87 Even, F/F #14	22	W/BL
	15	J19-3		Bit #86 Odd, F/F #15	22	V
	16	J19-C		Bit #86 Even,F/F #16	22	W/V
	17	J19-2		Bit #85 Odd,F/F #17	22	S
	18	J19-B		Bit #85 Even,F/F #18	22	W/S
	19	J19-1		Bit #84 Odd, F/F#19	22	W
	20	J19-A		Bit #84 Even, F/F #20	22	BR/W
	21	J3-34		Core Driver Trigger	22	Y
	21	J2-34		Core Driver Trigger	22	Y

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 6 OF SHEETS

J2

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	22	J3-35	1	Odd Reset Trigger	22	O
	22	J2-35	1	Odd Reset Trigger	22	O
	23	J3-36	1	Even Reset Trigger	22	W/O
	23	J2-36	1	Even Reset Trigger	22	W/O
	24	J3-37	1	Odd FF Gate	22	G
	24	J2-37	1	Odd FF Gate	22	G
	25	J3-38	1	Even FF Gate	22	W/G
	25	J2-38	1	Even FF Gate	22	W/G
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J1-21	1	Core Driver Trigger	22	Y
	34	J2-21	1	Core Driver Trigger	22	Y
	35	J1-22	1	Odd Reset Trigger	22	O
	35	J2-22	1	Odd Reset Trigger	22	O
	36	J1-23	1	Even Reset Trigger	22	W/O
	36	J2-23	1	Even Reset Trigger	22	W/O
	37	J1-24	1	Odd F/F Gate	22	G
	37	J2-24	1	Odd F/F Gate	22	G
	38	J1-25	1	Even F/F Gate	22	W/G
	38	J2-25	1	Even F/F Gate	22	W/G

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 7 OF SHEETS

J2

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	39					
	40	J3-41	1	Core Output	22	W/BR
	41	J1-40	1	Core Input	22	BR
	42	J14-17V-4	2	-17V	20	W/S
	43	J14-17V-4	2	-17V	20	W/S
	44	+12V-4	2	+12V	20	R
	45	J14-0V-4	2	0V	20	BK
	46	J14-0V-4	2	0V	20	BK
	47	J14-20V-4	2	-20V	20	S
	48	J14-20V-4	2	-20V	20	S
	49	-85V-4	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 8 OF SHEETS

J3

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17-22	1	Bit #83 Odd, F/F #1	22	BK
	2	J18-22		Bit #83 Even, F/F #2	22	W/BK
	3	J17-U		Bit #82 Odd, F/F #3	22	BR
	4	J18-U		Bit #82 Even, F/F #4	22	W/BR
	5	J17-21		Bit #81 Odd, F/F #5	22	R
	6	J18-21		Bit #81 Even, F/F #6	22	W/R
	7	J17-T		Bit #80 Odd, F/F #7	22	O
	8	J18-T		Bit #80 Even, F/F #8	22	W/O
	9	J17-20		Bit #79 Odd, F/F #9	22	Y
	10	J18-20		Bit #79 Even, F/F #10	22	W/Y
	11	J17-S		Bit #78 Odd, F/F #11	22	G
	12	J18-S		Bit #78 Even, F/F #12	22	W/G
	13	J17-19		Bit #77 Odd, F/F #13	22	BL
	14	J18-19		Bit #77 Even, F/F #14	22	W/BL
	15	J17-R		Bit #76 Odd, F/F #15	22	V
	16	J18-R		Bit #76 Even, F/F #16	22	W/V
	17	J17-18		Bit #75 Odd, F/F #17	22	S
	18	J18-18		Bit #75 Even, F/F #18	22	W/S
	19	J17-Q		Bit #74 Odd, F/F #19	22	W
	20	J18-Q		Bit #74 Even, F/F #20	22	BR/W
	21	J4-34		Core Driver Trigger	22	Y
	21	J3-34		Core Driver Trigger	22	Y

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 9 OF SHEETS

J3

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	22	J4-35	1	Odd Reset Trigger	22	O
	22	J3-35	1	Odd Reset Trigger	22	O
	23	J4-36	1	Even Reset Trigger	22	W/O
	23	J3-36	1	Even Reset Trigger	22	W/O
	24	J4-37	1	Odd FF Gate	22	G
	24	J3-37	1	Odd FF Gate	22	G
	25	J4-38	1	Even FF Gate	22	W/G
	25	J3-38	1	Even FF Gate	22	W/G
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J2-21	1	Core Driver Trigger	22	Y
	34	J3-21	1	Core Driver Trigger	22	Y
	35	J2-22	1	Odd Reset Trigger	22	O
	35	J3-22	1	Odd Reset Trigger	22	O
	36	J2-23	1	Even Reset Trigger	22	W/O
	36	J3-23	1	Even Reset Trigger	22	W/O
	37	J2-24	1	Odd F/F Gate	22	G
	37	J3-24	1	Odd F/F Gate	22	G
	38	J2-25	1	Even F/F Gate	22	W/G
	38	J3-25	1	Even F/F Gate	22	W/G

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 10 OF SHEETS

J3
SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	39					
	40	J4-41	1	Core Output	22	BR
	41	J2-40	1	Core Input	22	W/BR
	42	J14+17V-5	2	-17V	20	W/S
	43	J14-17V-5	2	-17V	20	W/S
	44	+12V-5	2	+12V	20	R
	45	J14-0V-5	2	0V	20	BK
	46	J14-0V-5	2	0V	20	BK
	47	J14-20V-5	2	-20V	20	S
	48	J14-20V-5	2	-20V	20	S
	49	-85V-5	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 11 OF SHEETS

J4
SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17-17	1	Bit #73 Odd, F/F #1	22	BK
	2	J18-17		Bit #73 Even,F/F #2	22	W/BK
	3	J17-P		Bit #72 Odd, F/F #3	22	BR
	4	J18-P		Bit #72 Even, F/F #4	22	W/BR
	5	J17-16		Bit #71 Odd, F/F #5	22	R
	6	J18-16		Bit #71 Even, F/F #6	22	W/R
	7	J17-0		Bit #70 Odd, F/F #7	22	O
	8	J18-0		Bit #70 Even, F/F #8	22	W/O
	9	J17-15		Bit #69 Odd, F/F #9	22	Y
	10	J18-15		Bit #69 Even, F/F #10	22	W/Y
	11	J17-N		Bit #68 Odd, F/F #11	22	G
	12	J18-N		Bit #68 Even, F/F #12	22	W/G
	13	J17-14		Bit #67 Odd, F/F #13	22	BL
	14	J18-14		Bit #67 Even, F/F #14	22	W/BL
	15	J17-M		Bit #66 Odd, F/F #15	22	V
	16	J18-M		Bit #66 Even, F/F #16	22	W/V
	17	J17-13		Bit #65 Odd, F/F #17	22	S
	18	J18-13		Bit #65 Even, F/F #18	22	W/S
	19	J17-L		Bit #64 Odd, F/F #19	22	W
	20	J18-L		Bit #64 Even, F/F #20	22	BR/W
	21					
	22					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 12 OF SHEETS

J4

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	23					
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J3-21	1	Core Driver Trigger	22	Y
	35	J3-22	1	Odd Reset Trigger	22	O
	36	J3-23	1	Even Reset Trigger	22	W/O
	37	J3-24	1	Odd F/F Gate	22	G
	38	J3-25	1	Even F/F Gate	22	W/G
	39					
	40	J5-41	1	Core Output	22	W/BR
	41	J3-40	1	Core Input	22	BR
	42	J14-17V-6	2	-17V	20	W/S
	43	J14-17V-6	2	-17V	20	W/S
	44	+12V-6	2	+12V	20	R

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 13 OF SHEETS

J4

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	45	J14-0V-6	2	0V	20	BK
	46	J14-0V-6	2	0V	20	BK
	47	J14-20V-6	2	-20V	20	S
	48	J14-20V-6	2	-20V	20	S
	49	-85V-6	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 14 OF SHEETS

J5 SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17-12	1	Bit #63 Odd, F/F #1	22	BK
	2	J18-12		Bit #63 Even, F/F #2	22	W/BK
	3	J17-K		Bit #62 Odd, F/F #3	22	BR
	4	J18-K		Bit #62 Even, F/F #4	22	W/BR
	5	J17-11		Bit #61 Odd, F/F #5	22	R
	6	J18-11		Bit #61 Even, F/F #6	22	W/R
	7	J17-J		Bit #60 Odd, F/F #7	22	O
	8	J18-J		Bit #60 Even, F/F #8	22	W/O
	9	J17-10		Bit #59 Odd, F/F #9	22	Y
	10	J18-10		Bit #59 Even, F/F #10	22	W/Y
	11	J17-I		Bit #58 Odd, F/F #11	22	G
	12	J18-I		Bit #58 Even, F/F #12	22	W/G
	13	J17-9		Bit #57 Odd, F/F #13	22	BL
	14	J18-9		Bit #57 Even, F/F #14	22	W/BL
	15	J17-H		Bit #56 Odd, F/F #15	22	V
	16	J18-H		Bit #56 Even, F/F #16	22	W/V
	17	J17-8		Bit #55 Odd, F/F #17	22	S
	18	J18-8		Bit #55 Even, F/F #18	22	W/S
	19	J17-G		Bit #54 Odd, F/F #19	22	W
	20	J18-G		Bit #54 Even, F/F #20	22	BR/W
	21	J1-34		Core Driver Trigger	22	Y
	21	J5-34		Core Driver Trigger	22	Y

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 15 OF SHEETS

J5 SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	22	J1-35	1	Odd Reset Trigger	22	O
	22	J5-35	1	Odd Reset Trigger	22	O
	23	J1-36	1	Even Reset Trigger	22	W/O
	23	J5-36	1	Even Reset Trigger	22	W/O
	24	J1-37	1	Odd FF Gate	22	G
	24	J5-37	1	Odd FF Gate	22	G
	25	J1-38	1	Even FF Gate	22	W/G
	25	J5-38	1	Even FF Gate	22	W/G
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J6-21	1	Core Driver Trigger	22	Y
	34	J5-21	1	Core Driver Trigger	22	Y
	35	J6-22	1	Odd Reset Trigger	22	O
	35	J5-22	1	Odd Reset Trigger	22	O
	36	J6-23	1	Even Reset Trigger	22	W/O
	36	J5-23	1	Even Reset Trigger	22	W/O
	37	J6-24	1	Odd F/F Gate	22	G
	37	J5-24	1	Odd F/F Gate	22	G
	38	J6-25	1	Even F/F Gate	22	W/G
	38	J5-25	1	Even F/F Gate	22	W/G
	39					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 16 OF SHEETS

J5

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	40	J6-41	1	Core Output	22	BR
	41	J4-40	1	Core Input	22	W/BR
	42	J14-17V-7	2	-17V	20	W/S
	43	J14-17V-7	2	-17V	20	W/S
	44	+12V-7	2	+12V	20	R
	45	J14-0V-7	2	0V	20	BK
	46	J14-0V-7	2	0V	20	BK
	47	J14-20V-7	2	-20V	20	S
	48	J14-20V-7	2	-20V	20	S
	49	-85V-7	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 17 OF SHEETS

J6

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17-7	1	Bit #53 Odd, F/F #1	22	BK
	2	J18-7		Bit #53 Even, F/F #2		W/BK
	3	J17-F		Bit #52 Odd, F/F #3		BR
	4	J18-F		Bit #52 Even, F/F #4		W/BR
	5	J17-6		Bit #51 Odd, F/F #5		R
	6	J18-6		Bit #51 Even, F/F #6		W/R
	7	J17-E		Bit #50 Odd, F/F #7		O
	8	J18-E		Bit #50 Even, F/F #8		W/O
	9	J17-5		Bit #49 Odd, F/F #9		Y
	10	J18-5		Bit #49 Even, F/F #10		Y/W
	11	J17-D		Bit #48 Odd, F/F #11		G
	12	J18-D		Bit #48 Even, F/F #12		W/G
	13	J17-4		Bit #47 Odd, F/F #13		BL
	14	J18-4		Bit #47 Even, F/F #14		W/BL
	15	J17-C		Bit #46 Odd, F/F #15		V
	16	J18-C		Bit #46 Even, F/F #16		W/V
	17	J17-3		Bit #45 Odd, F/F #17		S
	18	J18-3		Bit #45 Even, F/F #18		W/S
	19	J17-B		Bit #44 Odd, F/F #19		W
	20	J18-B		Bit #44 Even, F/F #20		BR/W
	21	J5-34		Core Driver Trigger		Y
	21	J6-34		Core Driver Trigger		Y

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 18 OF SHEETS

J6

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	22	J5-35	1	Odd Reset Trigger	22	O
	22	J6-35	1	Odd Reset Trigger	22	O
	23	J5-36	1	Even Reset Trigger	22	W/O
	23	J6-36	1	Even Reset Trigger	22	W/O
	24	J5-37	1	Odd F/F Gate	22	G
	24	J6-37	1	Odd F/F Gate	22	G
	25	J5-38	1	Even F/F Gate	22	W/G
	25	J6-38	1	Even F/F Gate	22	W/G
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J9 -18	1	Core Driver Trigger	22	Y
	34	J6-21	1	Core Driver Trigger	22	Y
	35	J9 -13	1	Odd Reset Trigger	22	O
	35	J6-22	1	Odd Reset Trigger	22	O
	36	J9 -11	1	Even Reset Trigger	22	W/O
	36	J6-23	1	Even Reset Trigger	22	W/O
	37	J9 -14	1	Odd F/F Gate	22	G
	37	J6-24	1	Odd F/F Gate	22	G
	38	J9 - 12	1	Even F/F Gate	22	W/G
	38	J6-25	1	Even F/F Gate	22	W/G
	39					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 79WL1A | SHEET 19 OF SHEETS

J6

SHIFT REGISTER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	40	J9 -9	1	Core Output	22	W/BR
	41	J5-40	1	Core Input	22	BR
	42	J14-17V-8	2	-17V	20	W/S
	43	J14-17V-8	2	-17V	20	W/S
	44	+12V-8	2	+12V	20	R
	45	J14-0V-8	2	0V	20	BK
	46	J14-0V-8	2	0V	20	BK
	47	J14-20V-8	2	-20V	20	S
	48	J14-20V-8	2	-20V	20	S
	49	-85V-8	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 79WL1A | SHEET 20 OF SHEETS

J9

CONTROL CHASSIS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J20-D	1	Select & Ready	RG174/U	
	2	J9-46	Jumper	Coax Shield Bus		
	3	J20-B	1	Data	RG174/U	
	4					
	5	J20-H		Sample	RG174/U	
	6					
	7	J18-2		Bit #43 Even	22	W/R
	8	J17-2		Bit #43 Odd	22	R
	9	J6-40		Core Output from SR#6	22	W/BR
	10					
	11	J6-36		Even Reset Trigger	22	W/O
	12	J6-38		Even FF Gate	22	W/G
	13	J6-35		Odd Reset Trigger	22	O
	14	J6-37		Odd FF Gate	22	G
	15	J16-D		S & R to D/A	RG174/U	
	16					
	17	J20=F		D/A - T/R Ready	RG174/U	
	18	J6-34		Core Driver Trigger	22	Y
	19					
	20	J16=K		Sample to D/A	RG174/U	
	21					
	22	J16-B	1	Data to D/A	RG174/U	

NOTES: All Coax shields tie to chassis ground on one end only

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 21 OF SHEETS

J9

CONTROL CHASSIS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	23					
	24	J16-H	1	D/A Ready	RG174/U	
	25					
	26					
	27	J17-V	1	Odd Frame	22	W/BK
	28					
	29	J18-V	1	Even Frame	22	W/Y
	30					
	31	J21-B	1	Timing	RG174/U	
	32	J21-C	1	Timing Ret'n	RG174/U	
	33					
	34	J1-41	1	Core Input SR#1	22	W/BR
	35					
	36					
	37			AC Common		
	38	TB2-3	2	AC Common	20	W
	39	K1-1	2	$\emptyset_1$ Switched	20	S
	40	J14-17V-9	2	-17V	20	W/S
	41			Contactor Coil AC Common Sw.		
	42	K1-A	2	Contactor Coil AC Common Sw.	20	W

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 22 OF SHEETS

J9

CONTROL CHASSIS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	43	+12V-9	2	+12V	20	R
	44	+12V-10	2	+12V	20	R
	45	0V-3	2	0V	20	BK
	46	0V-4	2	0V	20	BK
	47	J14-20V-9	2	-20V	20	S
	48	J14-20V-9	2	-20V	20	S
	49	-85V-9	2	-85V	22	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 23 OF SHEETS

J11
CONTROL CHASSIS
POWER SUPPLY 165-4C

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	TB2-6	2	AC Common, 120V	18	W
	1	J11-2	Jumper			
	2	J11-1	Jumper			
	3					
	4	K1-2	2	Switched AC 120V	18	S
	4	J11-5	Jumper			
	5	J11-4	Jumper			
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 24 OF SHEETS

J11
CONTROL CHASSIS
POWER SUPPLY 165-4C

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V Bus-1	2	+12V Supply	20	R
	45	OV Bus-1	2	OV Supply	20	BK
	46	OV Bus-2	2	OV Supply	20	BK
	47					
	48					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 25 OF SHEETS

J11
CONTROL CHASSIS
POWER SUPPLY 165-4C

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	49	-85V Bus-1	2	-85V Supply	20	W/BK
	50	Frame		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 26 OF SHEETS

J14 OV BUS
S.R. POWER SUPPLY
76-9A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17--	1	0V	20	BK
	1	J18-+	1	0V	20	BK
	2	J18--	1	0V	20	BK
	2	J19-+	1	0V	20	BK
	3	J1-45	2	0V	20	BK
	3	J19--	1	0V	20	BK
	3	J1-46	2	0V	20	BK
	4	J2-45	2	0V	20	BK
	4	J17-+	1	0V	20	BK
	4	J2-46	2	0V	20	BK
	5	J3-45	2	0V	20	BK
	5	J3-46	2	0V	20	BK
	6	J4-45	2	0V	20	BK
	6	J4-46	2	0V	20	BK
	7	J5-45	2	0V	20	BK
	7	J5-46	2	0V	20	BK
	8	J6-45	2	0V	20	BK
	8	J6-46	2	0V	20	BK
	9	J20-G	1	0V	20	BK
	10	0V-10	2	0V Common	18	BK
	11	J21-A	1	0V	20	BK
	12	J16-J	1	0V	20	BK

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 27 OF SHEETS

J14 -17V BUS
S.R. SUPPLY 76-9A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3	J1-42	2	-17V	20	W/S
	3	J1-43				
	4	J2-42				
	4	J2-43				
	5	J3-42				
	5	J3-43				
	6	J4-42				
	6	J4-43				
	7	J5-42				
	7	J5-43				
	8	J6-42				
	8	J6-43				
	9	J9-40	2	-17V	20	W/S
	10					
	11					
	12					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 28 OF SHEETS

J14 -20V BUS
SR. POWER SUPPLY
76-9A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3	J1-47	2	-20V	20	S
	3	J1-48				
	4	J2-47				
	4	J2-48				
	5	J3-47				
	5	J3-48				
	6	J4-47				
	6	J4-48				
	7	J5-47				
	7	J5-48				
	8	J6-47				
	8	J6-48				
	9	J9-47				
	9	J9-48	2	-20V	20	S
	10					
	11					
	12					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 29 OF SHEETS

J15
AC POWER CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S1-1	3	120VAC $\emptyset_1$ Input	12	W/S
	C	S1-4	3	AC Neutral Input	12	W

NOTES: Connector Type MS3102A-18-10P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 30 OF SHEETS

J16

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A					
	B	J9-22	1	Data to D/A	RG174/U	
	C					
	D	J9-15	1	S & R to D/A	RG174/U	
	E					
	F			Coax Shields		
	G					
	H	J9-24	1	D/A Ready	RG174/U	
	J	J14-0V-12	1	0V	20	BK
	K	J9-20	1	Sample to D/A	RG174/U	
	L					
	M					
	N					
	P					
	R					
	S					
	T					
	U					
	V					

NOTES
Connector Type MS3102A-22-14P
Tie Coax Shields to Pin F.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A | 79WL1A | SHEET 31 OF SHEETS

J17

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	A					
	2	J9-8	1	Bit #43 Odd	22	R
	B	J6-19	1	Bit #44 Odd, F/F #19-6	22	W
	3	J6-17		Bit #45 Odd, F/F #17-6	22	S
	C	J6-15		Bit #46 Odd, F/F #15-6	22	V
	4	J6-13		Bit #47 Odd, F/F #13-6	22	BL
	D	J6-11		Bit #48 Odd, F/F #11-6	22	G
	5	J6-9		Bit #49 Odd, F/F #9-6	22	Y
	E	J6-7		Bit #50 Odd, F/F #7-6	22	O
	6	J6-5		Bit #51 Odd, F/F #5-6	22	R
	F	J6-3		Bit #52 Odd, F/F #3-6	22	BR
	7	J6-1		Bit #53 Odd, F/F #1-6	22	BK
	G	J5-19		Bit #54 Odd, F/F #19-5	22	W
	8	J5-17		Bit #55 Odd, F/F #17-5	22	S
	H	J5-15	1	Bit #56 Odd, F/F #15-5	22	V
	9	J5-13		Bit #57 Odd, F/F #13-5	22	BL
	I	J5-11		Bit #58 Odd, F/F #11-5	22	G
	10	J5-9		Bit #59 Odd, F/F #9-5	22	Y
	J	J5-7		Bit #60 Odd, F/F #7-5	22	O
	11	J5-5	1	Bit #61 Odd, F/F #5-5	22	R

NOTES:
CONNECTOR TYPE MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A | 79WL1A | SHEET 32 OF SHEETS

J17

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	K	J5-3	1	Bit #62 Odd, F/F #3-5	22	BR
	12	J5-1		Bit #63 Odd, F/F #1-5	22	BK
	L	J4-19		Bit #64 Odd, F/F #19-4	22	W
	13	J4-17		Bit #65 Odd, F/F #17-4	22	S
	M	J4-15		Bit #66 Odd, F/F #15-4	22	V
	14	J4-13		Bit #67 Odd, F/F #13-4	22	BL
	N	J4-11		Bit #68 Odd, F/F #11-4	22	G
	15	J4-9		Bit #69 Odd, F/F #9-4	22	Y
	O	J4-7		Bit #70 Odd, F/F #7-4	22	O
	16	J4-5		Bit #71 Odd, F/F #5-4	22	R
	P	J4-3		Bit #72 Odd, F/F #3-4	22	BR
	17	J4-1		Bit #73 Odd, F/F #1-4	22	BK
	Q	J3-19		Bit #74 Odd, F/F #19-3	22	W
	18	J3-17		Bit #75 Odd, F/F #17-3	22	S
	R	J3-15		Bit #76 Odd, F/F #15-3	22	V
	19	J3-13		Bit #77 Odd, F/F #13-3	22	BL
	S	J3-11		Bit #78 Odd, F/F #11-3	22	G
	20	J3-9		Bit #79 Odd, F/F #9-3	22	Y
	T	J3-7		Bit #80 Odd, F/F #7-3	22	O
	21	J3-5		Bit #81 Odd, F/F #5-3	22	R
	U	J3-3		Bit #82 Odd, F/F #3-3	22	BR
	22	J3-1		Bit #83 Odd, F/F #1-3	22	BK
	V	J9-27	1	Odd Frame	22	W/BK

NOTES:
CONNECTOR TYPE MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 79WL1A | SHEET 33 OF SHEETS

J17

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	W					
	23					
	X					
	24					
	Y					
	25					
	+	J14-0V-4	1		20	BK
	-	J14-0V-1	1		20	BK

NOTES: Connector Type
MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 79WL1A | SHEET 33A OF SHEETS

J18

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	A					
	2	J9-7	1	Bit #43 Even	22	W/R
	B	J6-20	1	Bit #44 Even, F/F #20-6	22	BR/W
	3	J6-18		Bit #45 Even, F/F #18-6	22	W/S
	C	J6-16		Bit #46 Even, F/F #16-6	22	W/V
	4	J6-14		Bit #47 Even, F/F #14-6	22	W/BL
	D	J6-12		Bit #48 Even, F/F #12-6	22	W/G
	5	J6-10		Bit #49 Even, F/F #10-6	22	Y/W
	E	J6-8		Bit #50 Even, F/F #8-6	22	W/O
	6	J6-6		Bit #51 Even, F/F #6-6	22	W/R
	F	J6-4		Bit #52 Even, F/F #4-6	22	W/BR
	7	J6-2		Bit #53 Even, F/F #2-6	22	W/BK
	G	J5-20		Bit #54 Even, F/F #20-5	22	BR/W
	8	J5-18		Bit #55 Even, F/F #18-5	22	W/S
	H	J5-16		Bit #56 Even, F/F #16-5	22	W/V
	9	J5-14		Bit #57 Even, F/F #14-5	22	W/BL
	I	J5-12		Bit #58 Even, F/F #12-5	22	W/G
	10	J5-10		Bit #59 Even, F/F #10-5	22	W/Y
	J	J5-8		Bit #60 Even, F/F #8-5	22	W/O
	11	J5-6		Bit #61 Even, F/F #6-5	22	W/R
	K	J5-4	1	Bit #62 Even, F/F #4-5	22	W/BR

NOTES:

CONNECTOR TYPE MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 34 OF SHEETS

J18

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	12	J5-2	1	Bit #63 Even, F/F #2-5	22	W/BK
	L	J4-20		Bit #64 Even, F/F #20-4	22	BR/W
	13	J4-18		Bit #65 Even, F/F #18-4	22	W/S
	M	J4-16		Bit #66 Even, F/F #16-4	22	W/V
	14	J4-14		Bit #67 Even, F/F #14-4	22	W/BL
	N	J4-12		Bit #68 Even, F/F #12-4	22	W/G
	15	J4-10		Bit #69 Even, F/F #10-4	22	W/Y
	O	J4-8		Bit #70 Even, F/F #8-4	22	W/O
	16	J4-6		Bit #71 Even, F/F #6-4	22	W/R
	P	J4-4		Bit #72 Even, F/F #4-4	22	W/BR
	17	J4-2		Bit #73 Even, F/F #2-4	22	W/BK
	Q	J3-20		Bit #74 Even, F/F #20-3	22	BR/W
	18	J3-18		Bit #75 Even, F/F #18-3	22	W/S
	R	J3-16		Bit #76 Even, F/F #16-3	22	W/V
	19	J3-14		Bit #77 Even, F/F #14-3	22	W/BL
	S	J3-12		Bit #78 Even, F/F #12-3	22	W/G
	20	J3-10		Bit #79 Even, F/F #10-3	22	W/Y
	T	J3-8		Bit #80 Even, F/F #8-3	22	W/O
	21	J3-6		Bit #81 Even, F/F #6-3	22	W/R
	U	J3-4		Bit #82 Even, F/F #4-3	22	W/BR
	22	J3-2	1	Bit #83 Even, F/F #2-3	22	W/BK
	V	J9-29	1	Even Frame	22	W/Y

NOTES:

CONNECTOR TYPE MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 35 OF SHEETS

J18

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	W					
	23					
	X					
	24					
	Y					
	25					
	+	J14-0V-1	1		20	BK
	-	J14-0V-2	1		20	BK

NOTES: Connector Type MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 35A OF SHEETS

J19

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J2-19	1	Bit #84 Odd, F/F #19-2	22	W
	A	J2-20		Bit #84 Even, F/F #20-2	22	BR/W
	2	J2-17		Bit #85 Odd, F/F #17-2	22	S
	B	J2-18		Bit #85 Even, F/F #18-2	22	W/S
	3	J2-15		Bit #86 Odd, F/F #15-2	22	V
	C	J2-16		Bit #86 Even, F/F #16-2	22	W/V
	4	J2-13		Bit #87 Odd, F/F #13-2	22	BL
	D	J2-14		Bit #87 Even, F/F #14-2	22	W/BL
	5	J2-11		Bit #88 Odd, F/F #11-2	22	G
	E	J2-12		Bit #88 Even, F/F #12-2	22	W/G
	6	J2-9		Bit #89 Odd, F/F #9-2	22	Y
	F	J2-10		Bit #89 Even, F/F #10-2	22	W/Y
	7	J2-7		Bit #90 Odd, F/F #7-2	22	O
	G	J2-8		Bit #90 Even, F/F #8-2	22	W/O
	8	J2-5		Bit #91 Odd, F/F #5-2	22	R
	H	J2-6		Bit #91 Even, F/F #6-2	22	W/R
	9	J2-3		Bit #92 Odd, F/F #3-2	22	BR
	I	J2-4		Bit #92 Even, F/F #4-2	22	W/BR
	10	J2-1		Bit #93 Odd, F/F #1-2	22	BK
	J	J2-2		Bit #93 Even, F/F #2-2	22	W/BK
	11	J1-19		Bit # 94 Odd, F/F #19-1	22	W
	K	J1-20	1	Bit #94 Even, F/F #20-1	22	BR/W

NOTES:

CONNECTOR TYPE MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 36 OF SHEETS

J19

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	12	J1-17	1	Bit #95 Odd, F/F#17-1	22	S
	L	J1-18		Bit #95 Even, F/F#18-1	22	W/S
	13	J1-15		Bit #96 Odd, F/F#15-1	22	V
	M	J1-16		Bit #96 Even, F/F #16-1	22	W/V
	14	J1-13		Bit #97 Odd, F/F #13-1	22	BL
	N	J1-14		Bit #97 Even, F/F #14-1	22	W/BL
	15	J1-11		Bit #98 Odd, F/F #11-1	22	G
	O	J1-12		Bit #98 Even, F/F #12-1	22	W/G
	16	J1-9		Bit #99 Odd, F/F #9-1	22	Y
	P	J1-10		Bit #99 Even, F/F #10-1	22	W/Y
	17	J1-7		Bit #100 Odd, F/F #7-1	22	O
	Q	J1-8		Bit #100 Even, F/F #8-1	22	W/O
	18	J1-5		Bit #101 Odd, F/F #5-1	22	R
	R	J1-6		Bit #101 Even, F/F #6-1	22	W/R
	19	J1-3		Bit #102 Odd, F/F #3-1	22	BR
	S	J1-4		Bit #102 Even, F/F #4-1	22	W/BR
	20	J1-1		Bit #103 Odd, F/F #1-1	22	BK
	T	J1-2	1	Bit #103 Even, F/F #2-1	22	W/BK

NOTES:
CONNECTOR TYPE MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 37 OF SHEETS

J19

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	W					
	23					
	X					
	24					
	Y					
	25					
	+	J14-0V-2	1		20	BK
	-	J14-0V-3	1		20	BK

NOTES: Connector Type
MS3102A-36-404P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 37A OF SHEETS

J20

INPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A					
	B	J9-3	1	Data	RG174/U	
	C					
	D	J9-1	1	Select & Ready	RG174/U	
	E					
	F	J9-17	1	D/A - T/R Ready	RG174/U	
	G	J14-9	1	0 Volts	20	BK
	H	J9-5	1	Sample	RG174/U	

NOTES:
Connector Type MS3102A-22-18P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 38 OF SHEETS

J21

OUTPUT CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J14-11	1	0 Volts	20	BK
	B	J9-31	1	Timing	RG174/U	
	C	J9-32	1	Timing Ret'n	RG174/U	
	D					

NOTES:
Connector Type MS-3102A-18-13P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 39 OF SHEETS

+12 VOLT BUS

C.C. SUPPLY 165-4C

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J11-44	2	+12V Supply	20	R
	2					
	3	J1-44	2	+12V	20	R
	4	J2-44	2	+12V	20	R
	5	J3-44	2	+12V	20	R
	6	J4-44	2	+12V	20	R
	7	J5-44	2	+12V	20	R
	8	J6-44	2	+12V	20	R
	9	J9-43	2	+12V	20	R
	10	J9-44	2	+12V	20	R
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 40 OF SHEETS

0 VOLT BUS

C.C. SUPPLY 165-4C

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J11-45	2	0V Supply	20	BK
	2	J11-46	2	0V Supply	20	BK
	3	J9-45	2	0V	20	BK
	4	J9-46	2	0V	20	BK
	5					
	6					
	7					
	8					
	9					
	10	J14-10	2	0V Common	18	BK
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 41 OF SHEETS

-85 VOLT BUS
C.C. SUPPLY 165-4C

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J11-49	2	-85V Supply	20	W/BK
	2					
	3	J1-49	2	-85V	22	W/BK
	4	J2-49	2	-85V	22	W/BK
	5	J3-49	2	-85V	22	W/BK
	6	J4-49	2	-85V	22	W/BK
	7	J5-49	2	-85V	22	W/BK
	8	J6-49	2	-85V	22	W/BK
	9	J9-49	2	-85V	22	W/BK
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

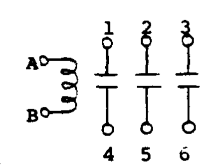
NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 42 OF SHEETS

K1 CONTACTOR
POWER PANEL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	K1-2	Jumper			
	1	J9-39	2	$\emptyset_1$ Switched Monitor	20	S
	1	TB1-1	2	Blower AC Switched	18	S
	2	K1-1	Jumper			
	2	K1-3	Jumper			
	2	J11-4	2	AC Switched (165-4C)	18	S
	3	K1-2	Jumper			
	3	T902-1	2	AC Switched (76-9A)	14	S
	4	K1-5	Jumper			
	4	K1-B	Jumper	Contactor Coil AC	20	S
	4	F1-2	2	$\emptyset_1$ Fused	12	S
	5	K1-4	Jumper			
	5	K1-6	Jumper			
	6	K1-5	Jumper			
	6	I_1-A	2	$\emptyset_1$ Indicator	20	S
	A	J9-42	2	Contactor Coil AC Common Sw.	20	W
	B	K1-4	Jumper	Contactor Coil AC	20	S



K1 Contactor

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 43 OF SHEETS

TB1

BLOWER TERM. BD.

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	K1-1	2	Ø1 Switched	18	S
	1	BL-1	2	Ø1 Switched	18	S
	2	TB2-5	2	Ø1 Return	18	W
	2	BL-2	2	Ø1 Return	18	W

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 44 OF SHEETS

BL BLOWER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	TB1-1	2	$Ø_1$ Switched	18	S
	2	TB1-2	2	$Ø_1$ Return	18	W

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 45 OF SHEETS

I_1 INDICATOR

POWER PANEL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	K1-6	2	$\emptyset_1$ Fused	20	S
	B	TB2-2	2	$\emptyset_1$ Return	20	W

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 46 OF SHEETS

F1 FUSE & F2 FUSE

POWER PANEL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	F1-1	S1-2	3	120VAC $\emptyset_1$ Hot	12	W/S
	F1-2	K1-4	2	$\emptyset_1$ Fused	12	S
	F2-1	S1-5	3	120VAC Neutral	12	W
	F2-2	TB2-1	2	120VAC Neutral Fused	12	W

F_1, F_2

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 47 OF SHEETS

S1 MAIN AC SWITCH

POWER PANEL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J15-A	3	120VAC $\emptyset_1$ Input	12	W/S
	2	F1-1	3	120VAC $\emptyset_1$ Hot	12	W/S
	3					
	4	J15-C	3	120VAC Neutral Input	12	W
	5	F2-1	3	120VAC Neutral	12	W
	6					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 48 OF SHEETS

TB2 NEUTRAL BUS

POWER PANEL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F2-2	2	120VAC Neutral Fuse	12	W
	2	I_1-B	2	Indicator Return	20	W
	3	J9-38	2	120V AC Common	20	W
	4					
	5	TB1-2	2	Blower Return	18	W
	6	J11-1	2	165-4C Supply Ret'n	18	W
	7	T902-2	2	76-9A Supply Ret'n	14	W
	8					
	9					
	10					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST A 79WL1A SHEET 49 OF SHEETS

T902

76-9A POWER SUPPLY

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	K1-3	2	AC Switched	14	S
	2	TB2-7	2	AC Return	14	W

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST

A 79WL1A
SHEET 50 OF 50 SHEETS

CHAPTER IX

SCHEMATICS AND DIAGRAMS

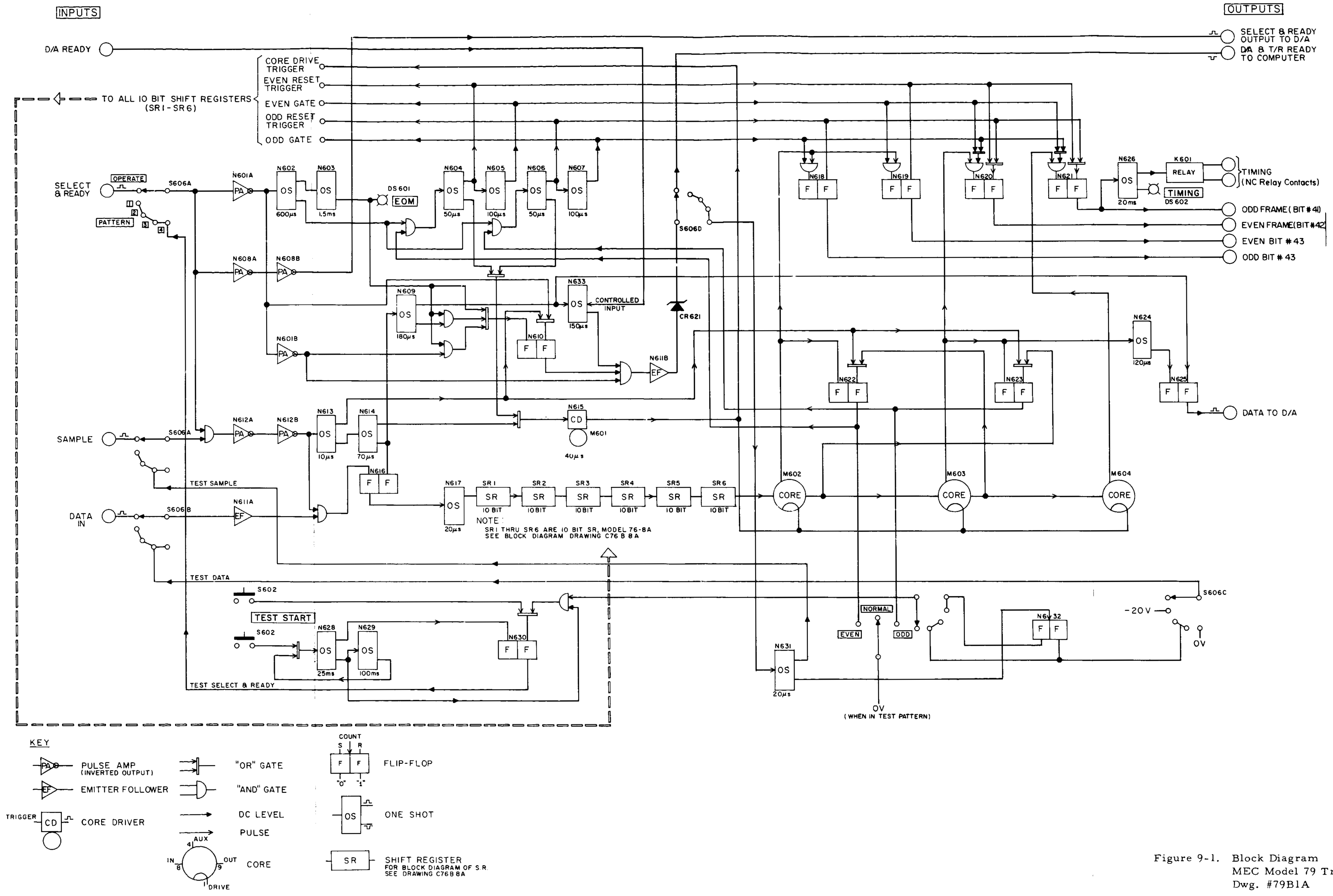


Figure 9-1. Block Diagram
MEC Model 79 Transfer Register
Dwg. #79B1A

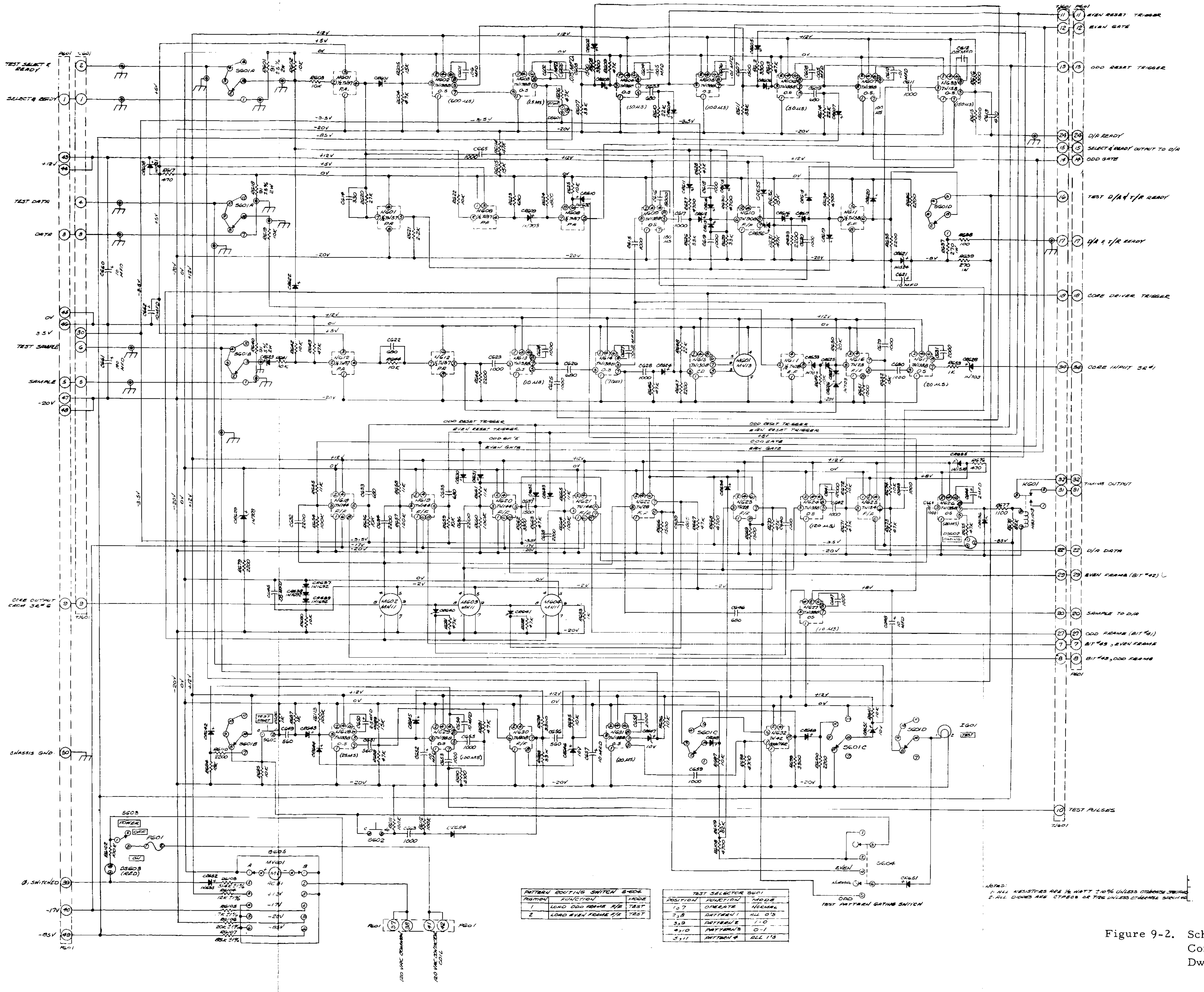


Figure 9-2. Schematic Control Chassis Dwg. #7956A

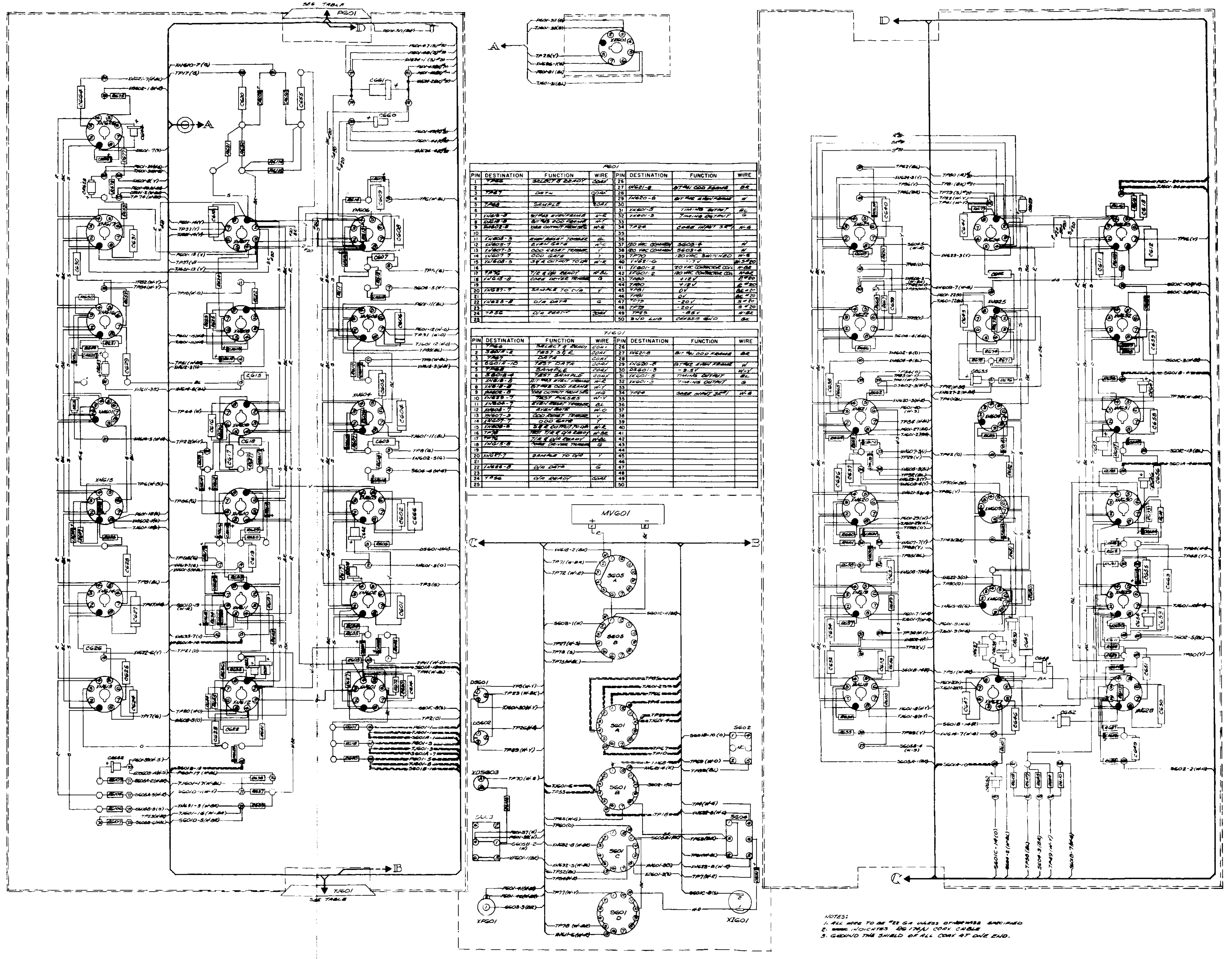
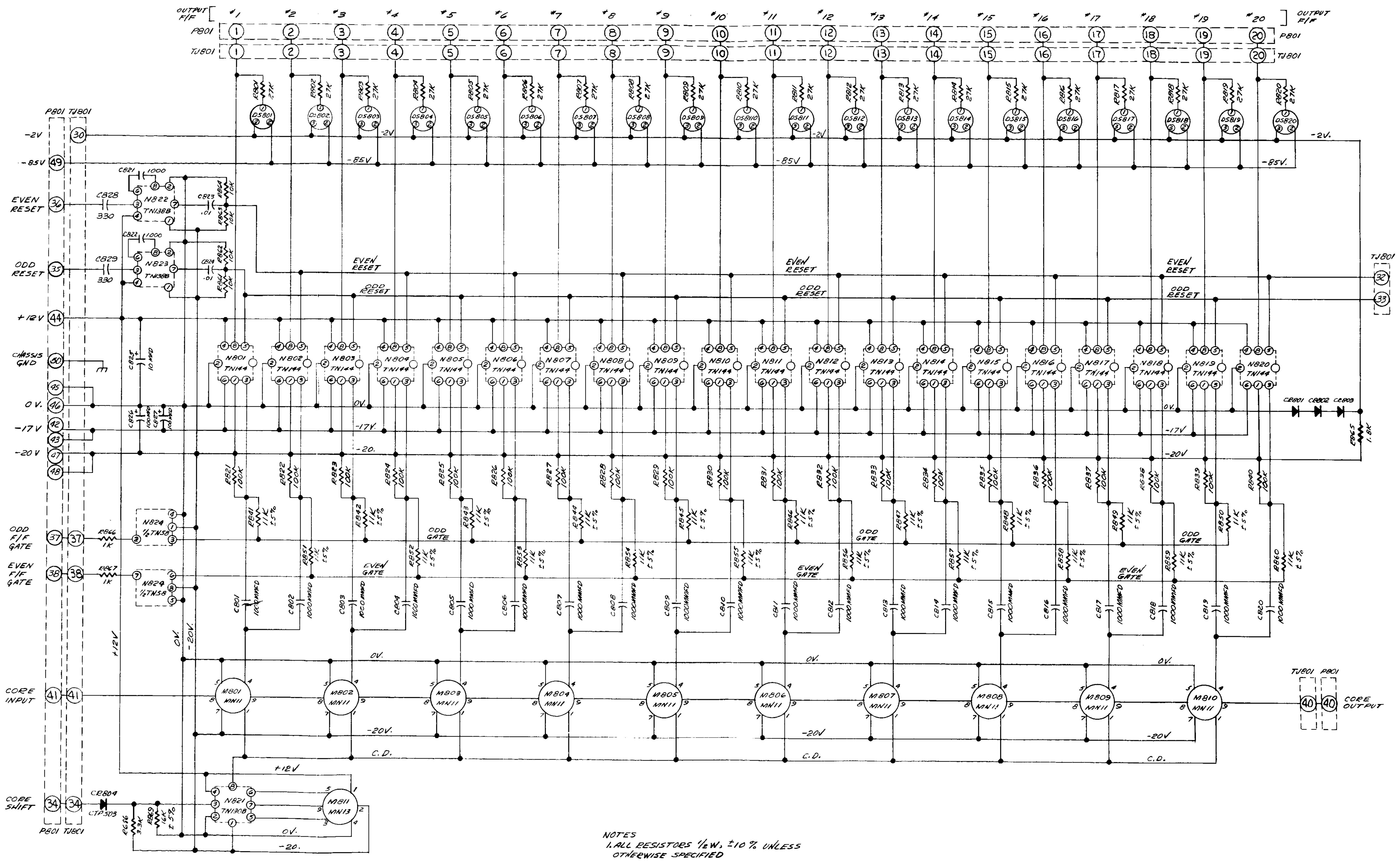
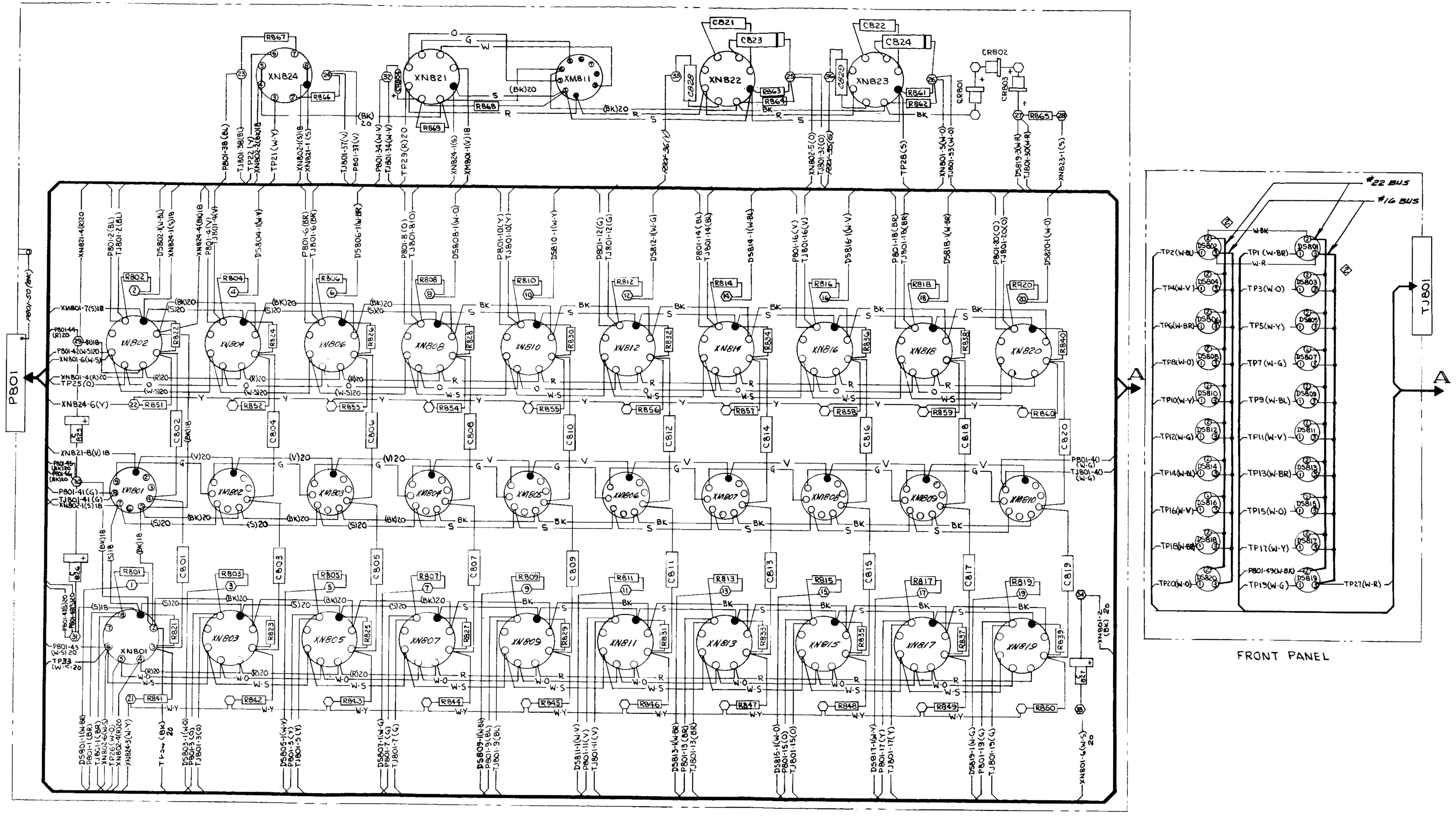


Figure 9-3. Wiring Diagram
Control Chassis
Dwg. #79W6A



NOTES
1. ALL RESISTORS 1/2W, ±10% UNLESS OTHERWISE SPECIFIED
2. CR801-CR803 ARE 1N1692

Figure 9-4. Schematic
10 Bit Shift Register
Dwg. #76S8A



P801											
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XN801-8	OUTPUT F/F	BR	18	XN818-8	OUTPUT F/F	BR	34	TP32	CORE SHIFT	W-V
2	XN802-8		BL	19	XN819-8		G	35	TP36	ODD RESET	G
3	XN803-8		O	20	XN820-8		O	36	TP35	EVEN RESET	Y
4	XN804-8		V	21				37	TP24	ODD GATE	V
5	XN805-8		Y	22				38	TP23	EVEN GATE	BL
6	XN806-8		BR	23				39			
7	XN807-8		G	24				40	XM810-9	CORE OUTPUT	W-G
8	XN808-8		O	25				41	XM801-6	CORE INPUT	G
9	XN809-8		BL	26				42	XN802-6	-17V	#20(W-S)
10	XN810-8		Y	27				43	XN801-6	-17V	#20(W-S)
11	XN811-8		V	28				44	TP29	+12V	#20(R)
12	XN812-8		G	29				45	TP30	0V	#20(BK)
13	XN813-8		BR	30				46	TP30	0V	#20(BK)
14	XN814-8		BL	31				47	TP31	-20V	#20(S)
15	XN815-8		C	32				48	TP31	-20V	#20(S)
16	XN816-8		V	33				49	DS819-2	-85V	W-BK
17	XN817-8		Y					50	GND. LUG	CHASSIS GND	BK

TJ801											
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XN801-8	OUTPUT F/F	BR	18	XN818-8	OUTPUT F/F	BR	34	TP32	CORE SHIFT	W-V
2	XN802-8		BL	19	XN819-8		G	35			
3	XN803-8		O	20	XN820-8		O	36			
4	XN804-8		V	21				37	TP-24	ODD F/F GATE	V
5	XN805-8		Y	22				38	TP-23	EVEN F/F GATE	BL
6	XN806-8		BR	23				39			
7	XN807-8		G	24				40	XM810-9	CORE OUTPUT	W-G
8	XN808-8		O	25				41	XM801-8	CORE INPUT	G
9	XN809-8		BL	26				42			
10	XN810-8		Y	27				43			
11	XN811-8		V	28				44			
12	XN812-8		G	29				45			
13	XN813-8		BR	30	TP27	-2V	W-R	46			
14	XN814-8		BL	31				47			
15	XN815-8		O	32	TP25	EVEN RESET	O	48			
16	XN816-8		V	33	TP26	ODD RESET	W-O	49			
17	XN817-8		Y					50			

Figure 9-5. Wiring Diagram
10 Bit Shift Register
Dwg. #76W8A

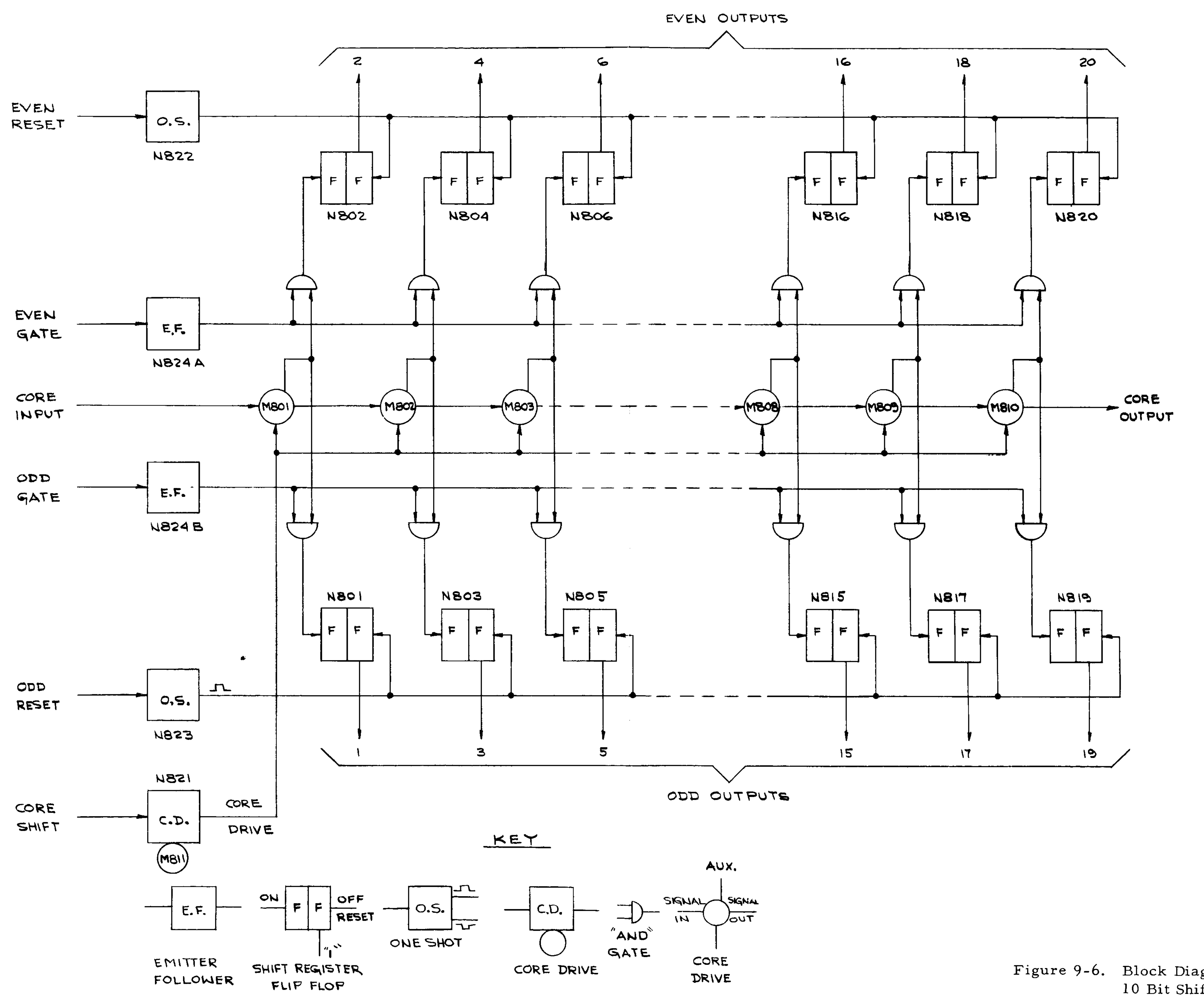
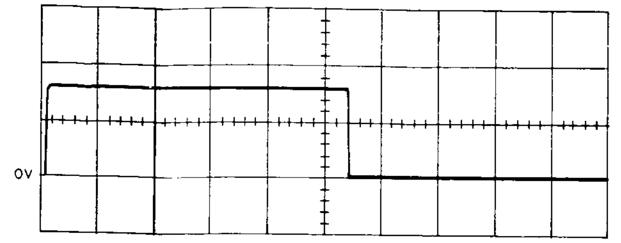
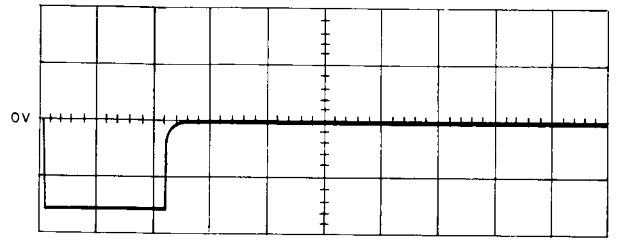


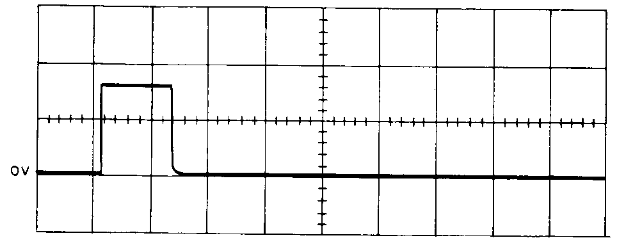
Figure 9-6. Block Diagram
10 Bit Shift Register
Dwg. #76B8A



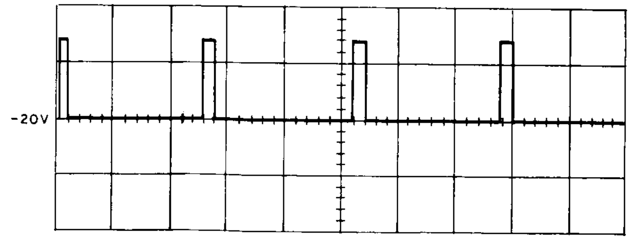
a. Select & Ready (TJ601-1
5v and 5MS/division
Sync internally (Int. plus)



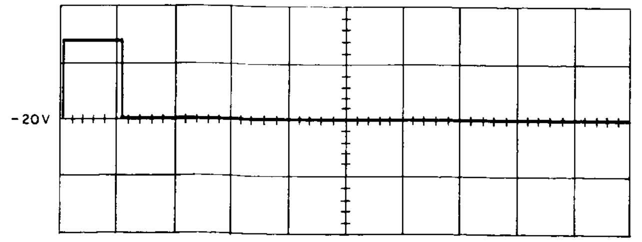
b. D/A-T/R Ready (TJ601-17)
5v and 5 micro S/division
Sync from TJ601-1 (Ext. plus)



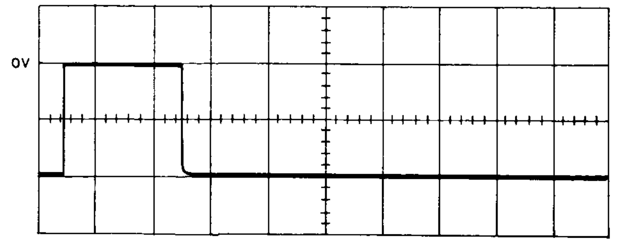
c. Sample (TJ601-5)
5v and 10 micro S/division
Sync from TJ6-1-1 (Ext. plus)



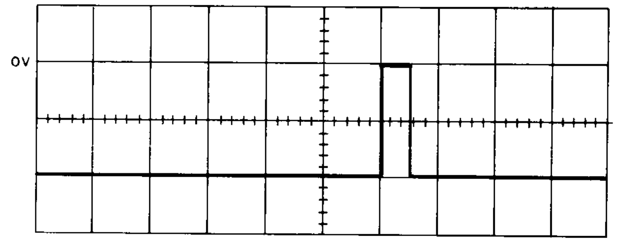
d. Core Input S. R. #1 (TJ601-34)
5v and 100 micro S/division
Sync from TJ601-5 (Ext. plus)



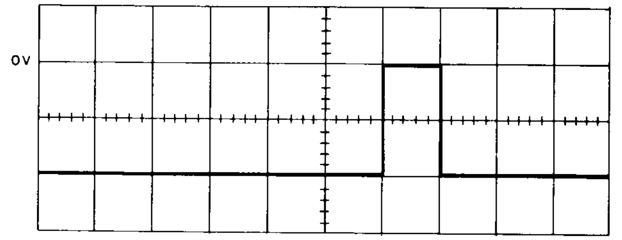
e. Core Input
5v and 20 micro S/division
Sync from TJ601-5 (Ext. plus)



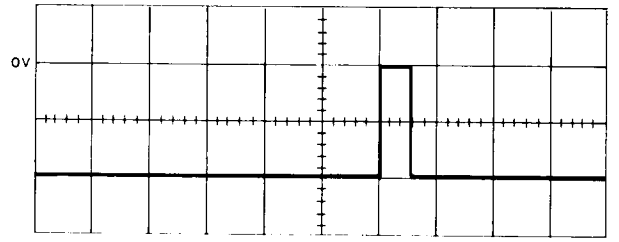
f. Core Driver Trigger
10v and 20 micro S/division
Sync from TJ601-5 (Ext. plus)



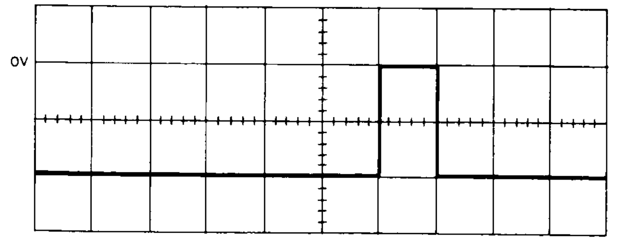
g. Even Reset Trigger
10v and 100 micro S/division
Sync from TJ601-1 (Ext. minus)



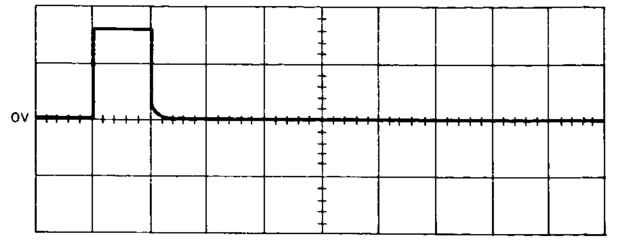
h. Even Gate (TJ601-12)
10v and 100 micro S/division
Sync from TJ601-1 (Ext. minus)



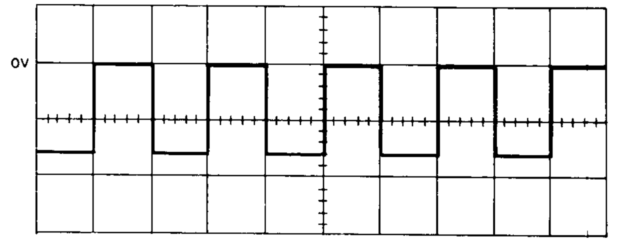
i. Odd Reset Trigger (TJ601-13)
10v and 100 micro S/division
Sync from TJ601-1 (Ext. minus)



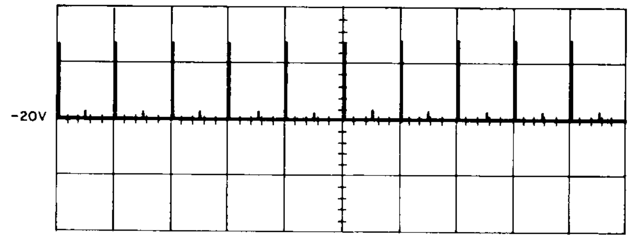
j. Odd Gate (TJ601-14)
10v and 100 micro S/division
Sync from TJ601-1 (Ext. minus)



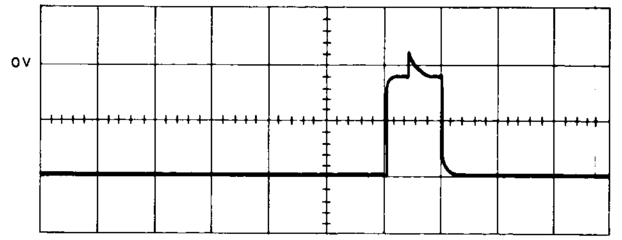
k. Sample to D-A
5v and 10 micro S/division
Sync from TJ601-5 (Ext. plus)



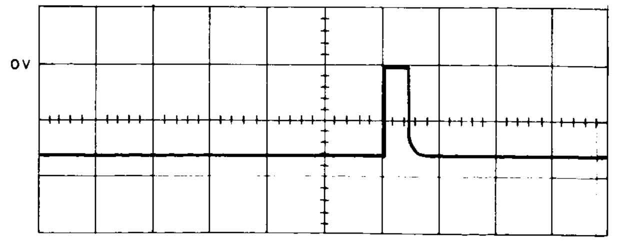
l. Odd Frame (Bit #41) Output (TJ601-27)
10v and 500 MS/division
Sync Internal (Int. minus)



m. Core Output from S. R. #6 ("1-0" pattern) - TJ601-9
5v and 500 micro S/division
Sync from TJ601-18 (Ext. plus)



n. Data Input to N801, pin 3 (N801-pin 3)
10v and 100 micro S/division
Sync from TJ601-1 (Ext. minus)



o. Data Output from N801 (TJ801-1)
10v and 100 micro S/division
Sync from TJ601-1 (Ext. minus)

Figure 9-7. Waveforms

CHAPTER X

APPENDIX

– 17 V AND – 20 V POWER SUPPLY

MEC MODEL 76-9 A

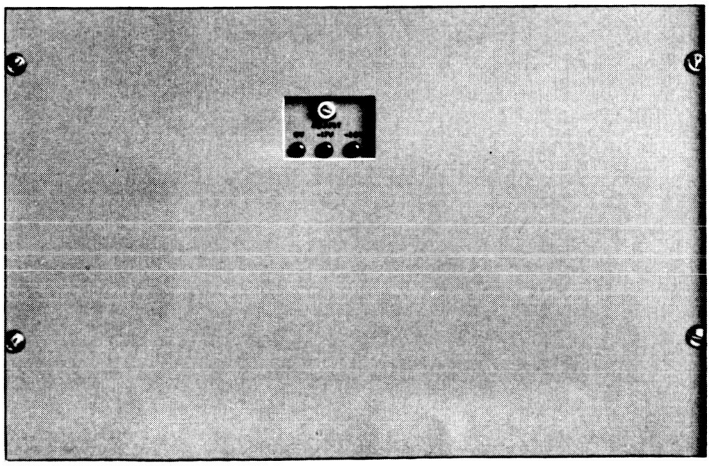
1. GENERAL

This power supply develops regulated output voltages of -17V at 40 amps and -20V at 3 amps. The -20V portion is developed by adding a -3V supply on the bottom of the -17V supply.

2. -17V SUPPLY

2-1. The 17V power supply is regulated by silicon controlled rectifiers (SCR) CR901 and CR902, by controlling the time which current can flow through their external circuit. When the external load is small, the SCRs are "on" for only a small amount of the input a-c cycle; when the external load is large, the SCRs are on for almost all of the input a-c cycle. The length of time which the SCRs are on is controlled by N901 (TN160) and its associated external circuitry.

2-2. CR901 and CR902 are SCRs which are phase-controlled elements used as a full wave rectifier element from the output of transformer T902. The two SCRs are fixed by gate signals from a common source, TN160. The operation of the circuit in TN160 is as follows: The unijunction transistor Q1 acts as a relaxation oscillator synchronized by its inter-base voltage supply. The firing circuit (TN160) is connected to the output of a single phase bridge formed by diodes CR904, CR905, CR906 and CR907, through R906. Zener diode (CR1) in the TN160 clips the rectified voltage, which charges capacitor C907 through resistor R7 in TN160. This voltage fires the unijunction transistor and whichever SCR has a positive anode voltage during that half cycle of the a-c input. Upon firing, the voltage across the SCRs decrease to the forward conduction value of less than 1 volt. This discharges capacitor C907, and keeps it discharged until the a-c input is reversed, at which time a new timing cycle starts for



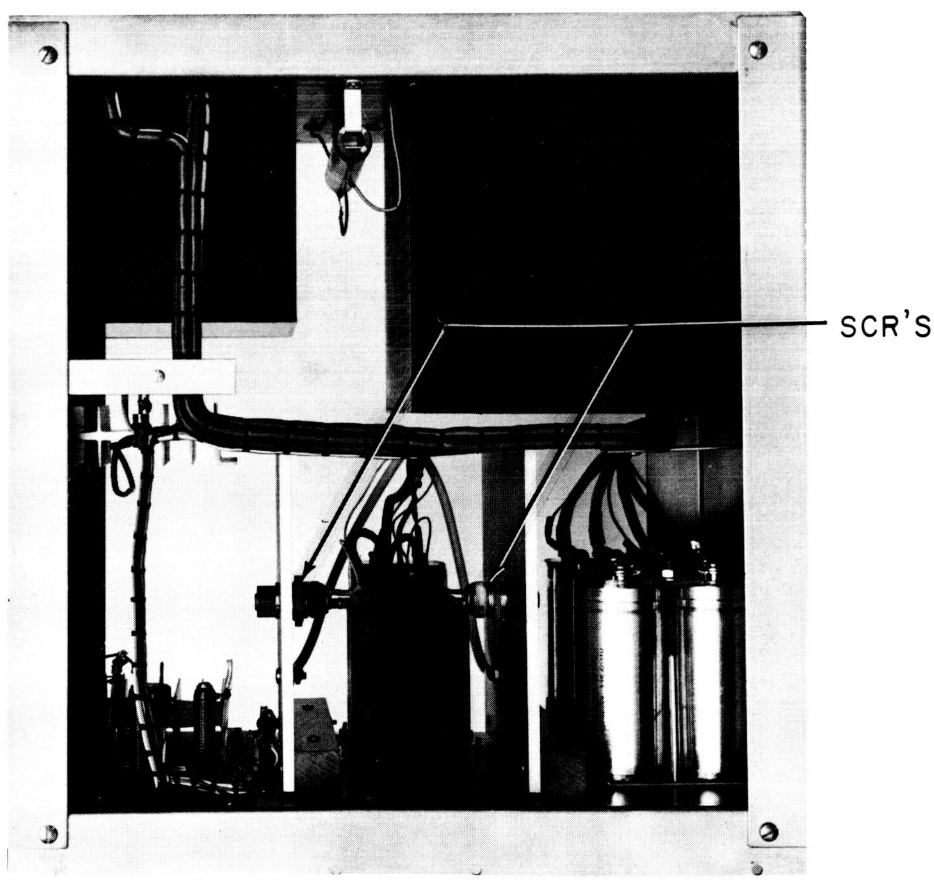
-17v and -20v Power Supply

the alternate SCR. If no current is being shunted by the voltage control circuit (Q2 and its associated circuitry) through R6, Q1 will fire within ten degrees after the beginning of each half cycle of the a-c supply voltage. At this minimum firing angle, the SCRs will deliver the maximum voltage to the load.

2-3. Q2 controls the firing angle by shunting C907. An increase of base current of Q2 will decrease the effective resistance of Q2, which will add a loading to C907, changing the charging time constant. This diversion of current will retard the firing angle so that a very small output will occur from CR901 and CR902.

2-4. DETAILED DESCRIPTION - The base current of Q2 is a feedback signal (or error voltage) developed from comparing a voltage on the base of Q2 (which is proportional to the output voltage) and a reference voltage across zener diode CR2 in the TN160. If the voltage tries to rise, more base current flows in Q2, resulting in more collector current. More collector current in Q2 will result in C907 taking longer to charge, and will therefore delay the time of the peak voltage on Q1.(the peak voltage on Q1 is the voltage necessary to fire Q1). This retards the firing angle and returns the output voltage to normal. If the output voltage drops, the reverse action takes place.

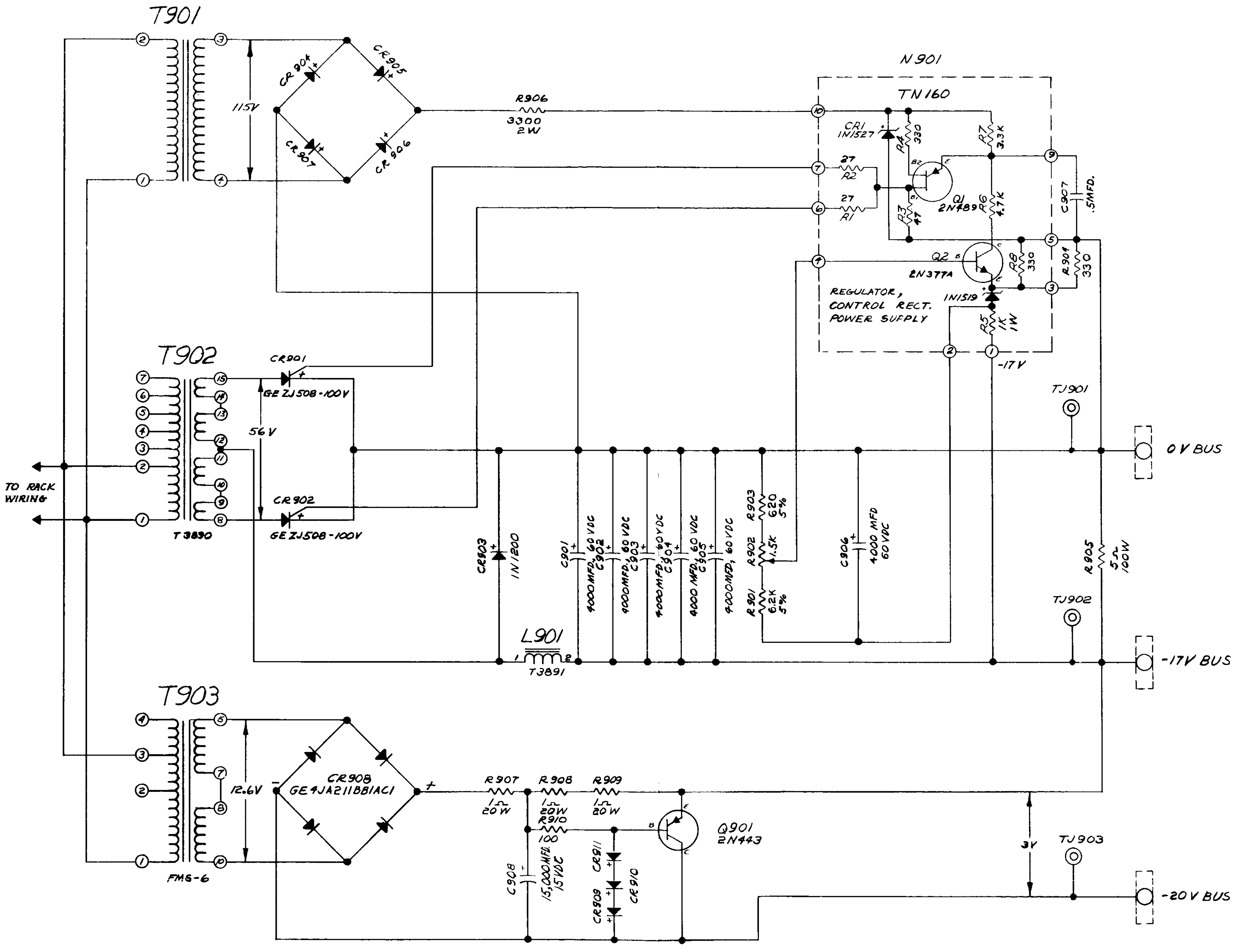
2-5. C906 and R5 are to increase stability in the feedback circuit. CR903 acts as a free wheeling diode to maintain current in the load and filter choke when the SCRs are both blocking. It contributes to over-all circuit stability. R905 is a minimum load. L901 and C901 through C905 are the filter section.



Power Supply, Bottom View, Showing Silicon-Controlled Rectifiers

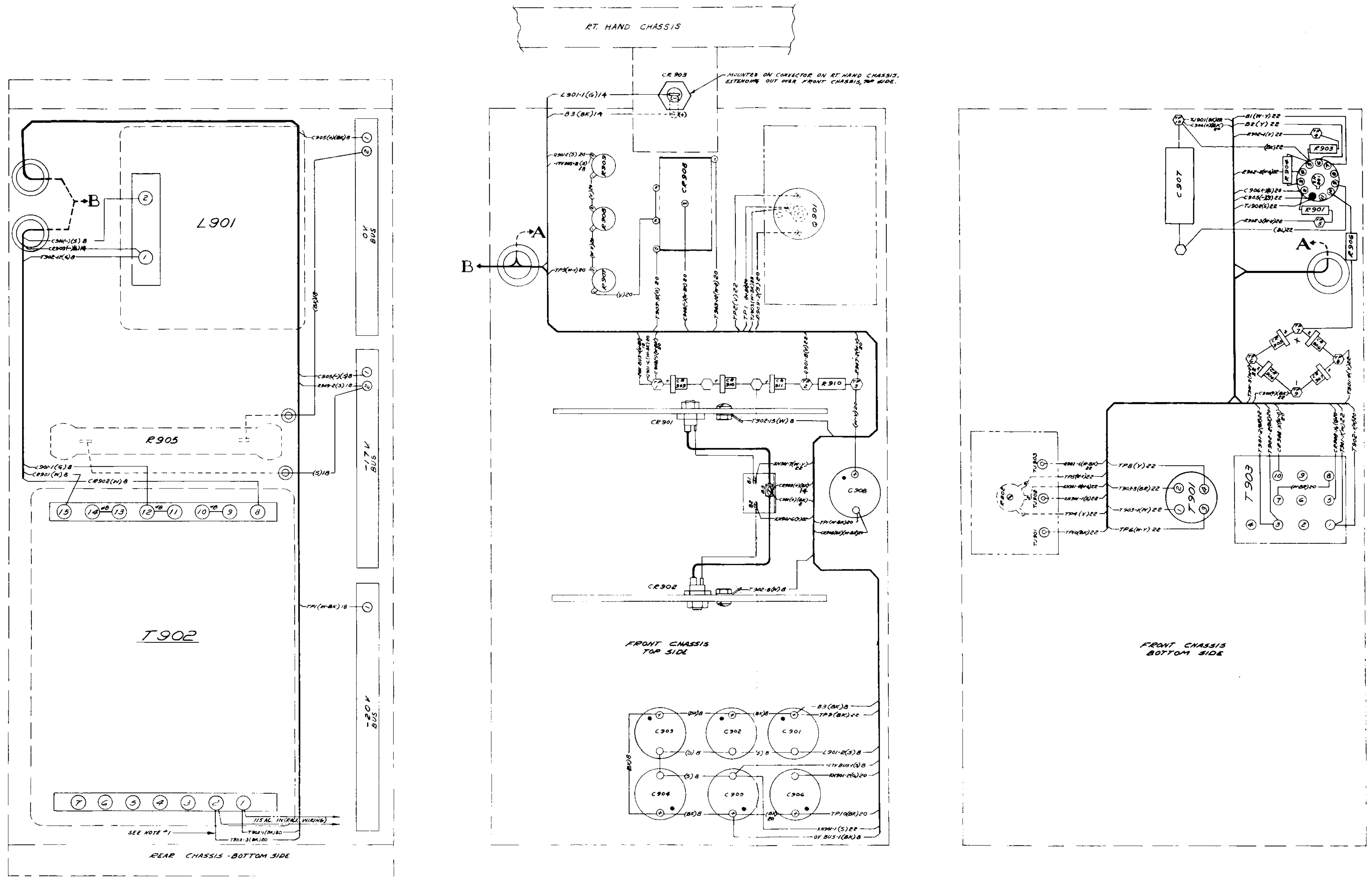
3. -20V SUPPLY

The -20V supply is only a -3V supply added on the bottom of the -17V supply. The voltage is rectified by CR908 and filtered by R907 and C908. Since the forward drop through silicon diodes are approximately constant through a large change of current, CR909, CR910 and CR911 are used as a voltage reference. Q901 acts as a shunt regulator, since its emitter voltage will be only about 0.3 volts from its base voltage, which is constant. Therefore the output voltage across Q901 is constant within the current rating of the supply. A constant current is flowing through R907, R908 and R909. When there is no external load, this current flows through Q901, but when there is an external load, current which flows through the external load is subtracted from the current flowing through Q901. R910 provides current for CR909, CR910 and CR911.



NOTES:
1. ALL RESISTORS ±10%, ½W UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES #1N1692 UNLESS OTHERWISE SPECIFIED.

Schematic
-20v, -17v Power Supply
Dwg. #C76S9A



NOTE:
1. LEAVE WIRES ON TERMINAL #2 LONG ENOUGH TO REACH TERMINAL #7

Wiring Diagram
-20v, -17v Power Supply
Dwg. #76W9A

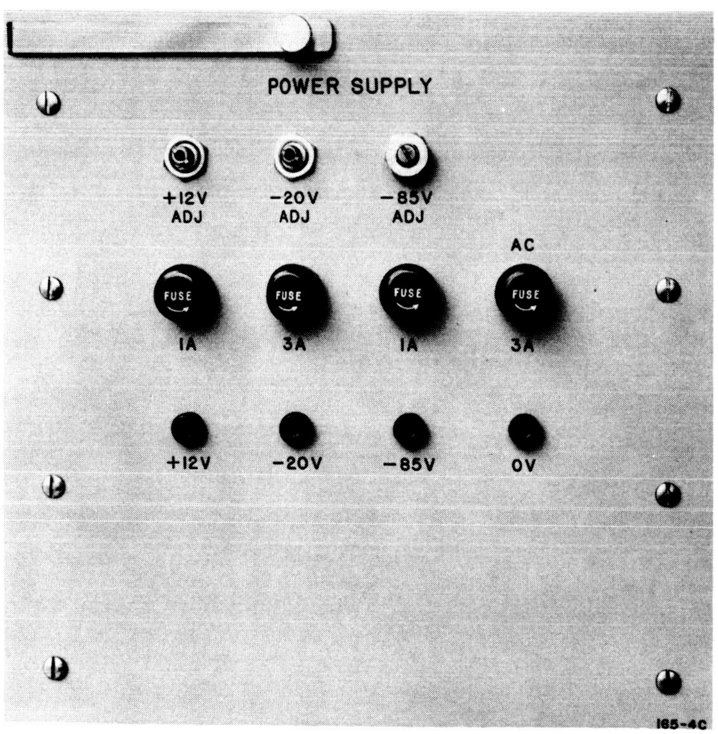
TRANSISTOR POWER SUPPLY
MEC MODEL 165-4 C

1. GENERAL DESCRIPTION

A Milgo type 165-4C Power Supply has three outputs: the first, a +12v, (+1v, -3v) at 1 ampere output; the second, a -20v, (+2v, -6v) at 2 amperes output; and the third, a -65v (±5v) at one ampere output. The -65v supply is stacked on the bottom of the -20v supply, thereby giving an output of -85v. The a-c input of this supply can vary from 100vac to 130vac and from 45 to 60 cycles. The unit is mounted in a standard Milgo slide-type rack and has a front panel 8-3/4 inches high by 8-7/8 inches wide. Its weight is approximately 35 pounds.

2. +12v SUPPLY

2-1. A portion of the output of transformer T401 is rectified by a bridge rectifier CR401 and filtered by resistor R401 and capacitors C401 and C402. The voltage across capacitors C401 and C402 is normally 20v (approximate). Transistor Q401 and resistors R402 and R403 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q401 is decreased so that the IR drop across R402, R403, and Q401 will remain constant producing a constant output voltage. If the input a-c line voltage should increase, the d-c voltage across filtered capacitors C401 and C402 would increase and the effective resistance of Q401 must increase again so that the output voltage will remain constant.



Transistor Power Supply

2-2. The effective resistance of Q401 is controlled by the control section, consisting of transistors Q402, Q403, Q404, and their associated circuitry. Q404 determines whether the output voltage is too high or too low and is followed by power amplifiers Q403 and Q402, which amplify the control signal to the necessary power level for driving Q401. The base voltage of Q404 is referenced from the output of 4.7v zener diode CR402. The emitter voltage of Q404 is determined by the resistor divider network of R413, R414,and R415. The voltage from the wiper of potentiometer R414 is applied to the emitter of Q404.

2-3. As the output voltage increases, the magnitude of the voltage from the wiper of R414 will also increase proportionally. Since the output across zener diode CR402 remains constant as the output voltage increases, the emitter voltage tends to go positive with respect to the base voltage, driving Q404 toward cutoff. As Q404 goes toward cutoff, there is less collector current through R410, so there is less base current in Q403. The emitter current of Q403 decreases, reducing the current through R407 and base current of Q402. With less base current in Q402, the emitter current decreases, reducing the base current of Q401. With less base current, the effective resistance of Q401 will increase. Therefore, the output voltage decreases until Q404 senses the correct relationship between the output voltage and the zener voltage of CR402.

2-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q404 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q404, which increases the base current of Q403, thus increasing the emitter current of Q403 and the base current of Q402. This in turn increases the emitter current of Q402 and the base current of Q401, which reduces the effective resistance of Q401, causing the output voltage to return to its regulated value. Q404 actually is matching the zener voltage to the emitter voltage.

2-5. Since a portion of the output voltage applied to the emitter of Q404 can be varied by potentiometer R414, and the emitter voltage of Q404 is to remain constant, the output voltage must be changed as the resistor R414 is changed. In this manner, the regulated output voltage can be adjusted over a range of +9v to +13v. Capacitor C403 has been added to prevent hunting. Resistors R402 and R403 are included to limit the peak current through transistor Q401 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q401 and Q402. Resistor R404 provides a path for the leakage current of Q402 so that this current does not affect the base current in Q401, allowing Q401 to be more nearly cut off during a light load.

3. -20v SUPPLY

3-1. A second portion of the output of transformer T401 is rectified by bridge rectifier CR421 and filtered by parallel resistors R421A and R421B, and capacitors C421, C422, and C423. The d-c voltage across capacitors C421, C422, and C423 is 30v (approximate). Transistors Q421 and Q422 with their associated resistors R423, R424, and R422 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q421 and Q422 is decreased so that the IR drop across R422, R423, R424, Q421, and Q422 will remain constant, producing a constant output voltage.

3-2. If the input a-c line voltage should increase, the d-c voltage across filter capacitors C421, C422, and C423 would increase, and the effective resistance of Q421 and Q422 must increase again to keep the output voltage constant. The effective resistance of Q421 and Q422 is controlled by the control section, consisting of transistors Q423, Q424, and Q425 and their associated circuitry. Transistor Q425 determines whether the output voltage is too high or too low and is followed by power amplifiers Q424 and Q423, which amplify the control signal to the necessary power level for driving Q421 and Q422. The base voltage of Q425 is referenced from the output by a 4.7v zener diode CR422. The emitter voltage of Q425 is determined by a resistor divider network R434, R435, and R436. The voltage from the wiper of potentiometer R435 is applied to the emitter of Q425.

3-3. As the output voltage increases, the magnitude of the voltage from the wiper of R435 will increase proportionally. Since the output across CR422 remains constant as the output voltage increases, the emitter voltage tends to become positive with respect to the base voltage, driving Q425, which is an NPN transistor, toward cutoff. As Q425 goes toward cutoff, there is less collector current through R431, and consequently, there is less base current in Q424. With less base current in Q424, the emitter current of Q424 decreases. With less emitter current in Q424, the current through R428 and the base current of Q423 also decrease. This reduces the emitter current in Q423 and reduces the base current in Q421 and Q422. Less base current in Q421 and Q422 increases their effective resistance, which increases the IR drop across them. Therefore, the output voltage decreases until Q425 senses the correct relationship between the output voltage and the zener voltage of CR422.

3-4. Conversely, if the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q425 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q425, increasing the base current of Q424, which in turn increases the emitter current of Q424 and the base current of Q423. This, in turn, increases the emitter current of Q423 and the base current of Q421 and Q422, reducing the effective resistance of Q421 and Q422, and causing the output voltage to return to its regulated value. Transistor Q425 is actually matching the zener voltage to the emitter voltage.

3-5. Since a portion of the output voltage applied to the emitter of Q425 can be varied by potentiometer R435, and the emitter voltage of Q425 is to remain constant, the output voltage will have to be changed as the resistor R435 is changed. In this manner, the regulated voltage of this supply can be adjusted from -14v to -22v. Capacitors C425 and C424 provide feedback for stabilization purposes.

3-6. Resistors R423 and R424 serve two functions. First, they force the collector current of Q421 and Q422 to balance. Since the bases are tied in common, if one transistor conducts more than the other, the higher IR drop in their associated resistor would tend to reverse bias the transistor with the most current and, in this manner, force the currents to balance. Second, if the output supply is shorted, resistors R422, R423 and R424 limit the peak current through Q421 and Q422 to a safe value while fuse F402 is melting. Resistor R425 provides a path for the leakage current of Q423 so that this leakage current does not affect the base current in Q421 and Q422. This allows Q421 and Q422 to be more nearly cut off during a light load.

4. -65v SUPPLY

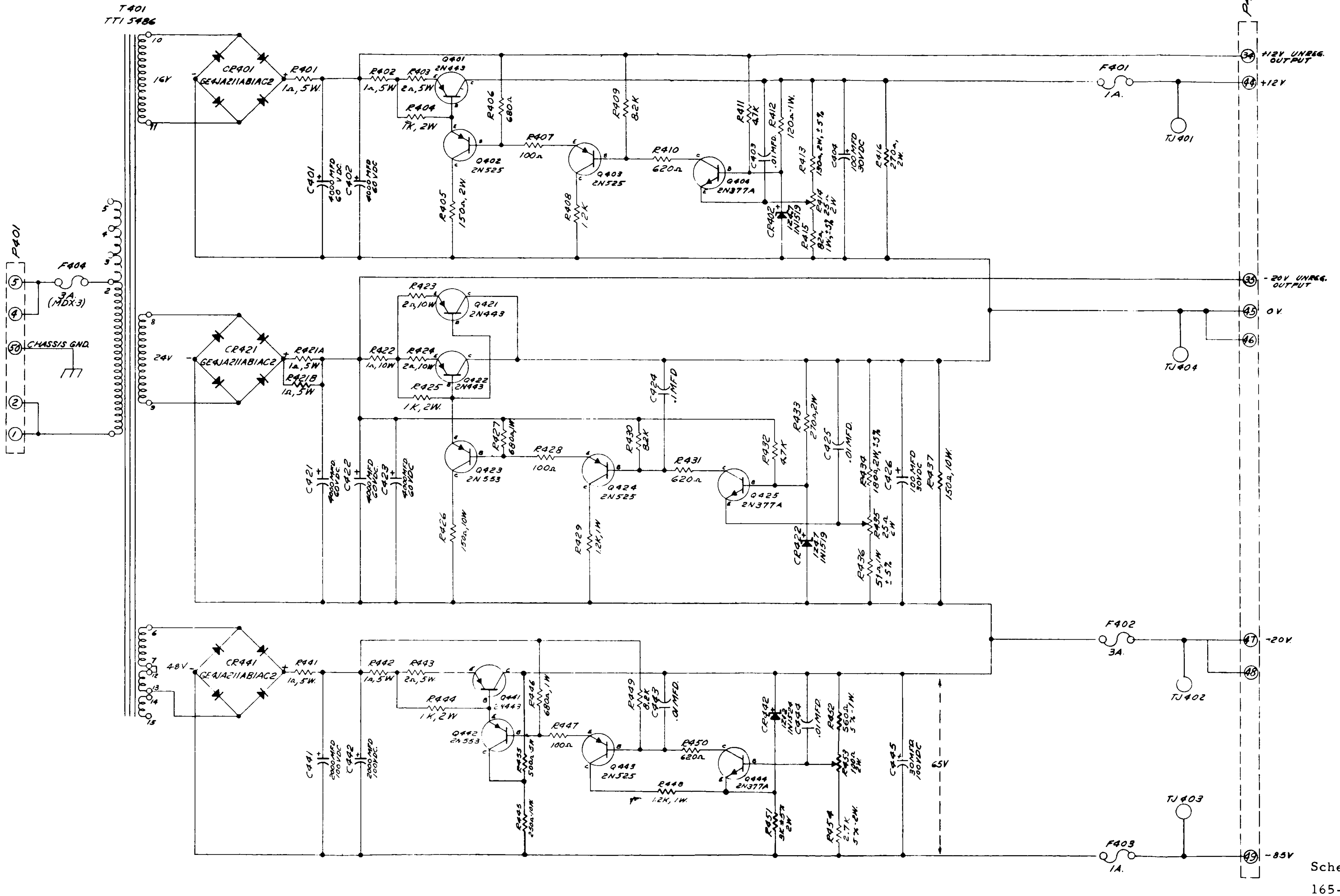
4-1. A third portion of the output of transformer T401 is rectified by a bridge rectifier CR441 and filtered by resistor R441 and capacitors C441 and C442. The voltage across capacitor C441 and C442 is normally 75v (approximate). Transistor Q441, and resistors R442 and R443, act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q441 is decreased so that the IR drop across R442, R443, and Q441 will remain constant, producing a constant output voltage. If the input a-c line voltage increases, the d-c voltage across filtered capacitors C441 and C442 will increase and the effective resistance of Q441 must increase again so that the output voltage will remain constant.

4-2. The effective resistance of Q441 is determined by the control section, consisting of transistors Q442, Q443, and Q444 and their associated circuitry. Q444 determines whether the output voltage is too high or too low and is followed by power amplifiers Q443 and Q442. These amplify the control signal to the necessary power level for driving Q441. The emitter voltage of Q444 is referenced from the output by a 12v zener diode CR442. The base voltage of Q444 is determined by the resistor divider network of R452, R453, and R454. The voltage from the wiper of potentiometer R453 is applied to the base of Q444. The zener is referenced from the positive side of this supply to reduce the emitter-to-collector voltage of Q443 and Q444 to less than 25v.

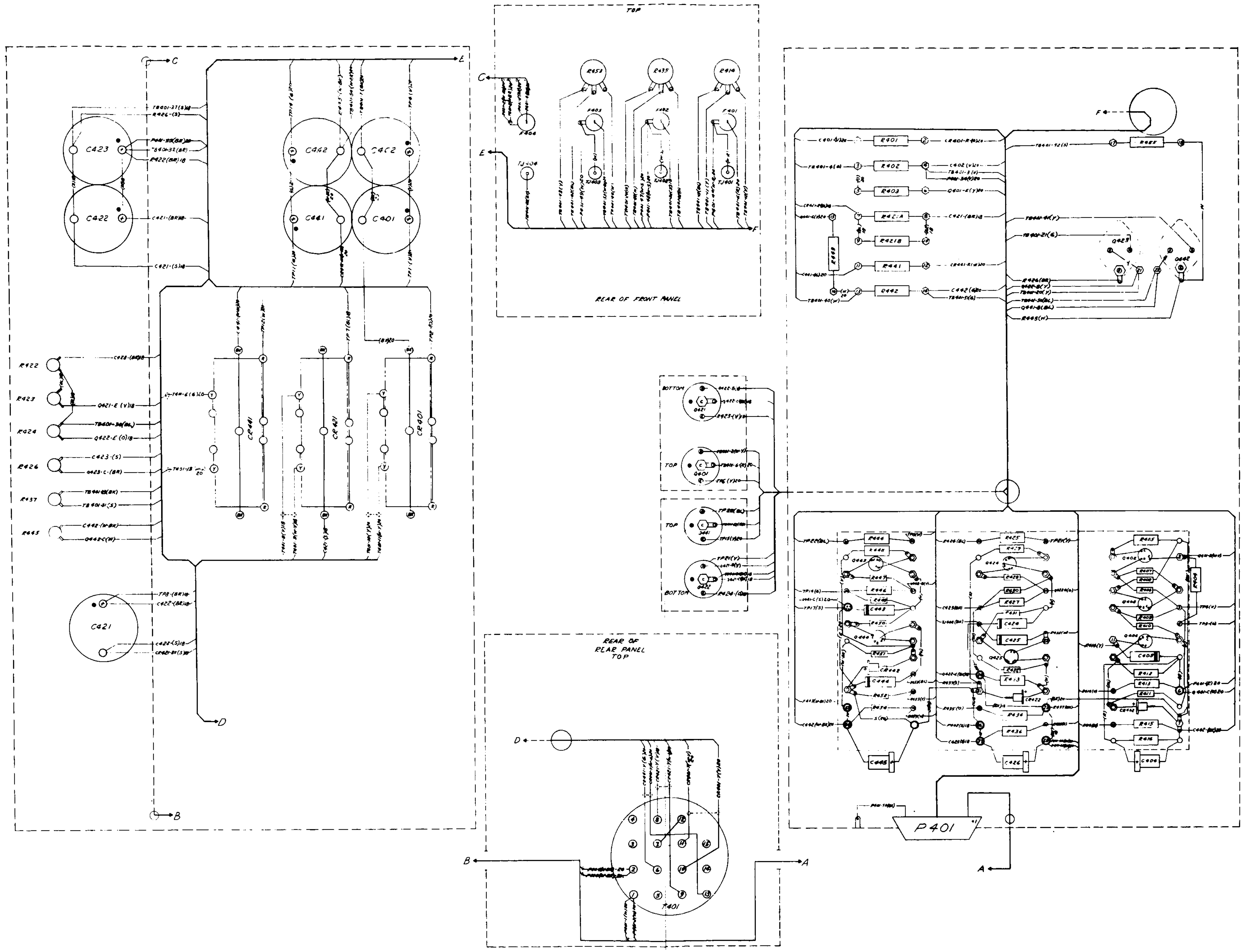
4-3. As the output voltage increases, the magnitude of the voltage from the wiper of R453 will also increase proportionally. Since the output across zener diode CR442 remains constant as the output volts increase, the base voltage tends to become negative with respect to the emitter voltage, driving Q444 toward cutoff. As Q444 goes toward cutoff, there is less collector current through R450 and less base current in Q443. The emitter current of Q443 decreases, reducing the current through R447 and the base current of Q442. With less base current, the Q442 emitter current decreases, reducing the base current of Q441. With less base current, the effective resistance of Q441 increases. Therefore, the output voltage decreases until Q444 senses the correct relationship between the output voltage and the zener voltage of CR442.

4-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the base of Q441 also decreases, tending to make the base more positive with respect to the emitter. This increases the collector current of Q444, increasing the base current of Q443, and increasing the emitter current of Q443 and the base current of Q442. This in turn increases the emitter current of Q442 and the base current of Q441, reducing the effective resistance of Q441, and causes the output voltage to increase and to return to its regulated value. Q444 is actually matching the zener voltage to the base voltage.

4-5. Since a portion of the output voltage applied to the base of Q444 can be varied by potentiometer R453, and the base voltage of Q444 is to remain constant, the output voltage will have to be changed as the resistor R453 is changed. In this manner, the regulated output voltage can be adjusted over a range of -60v to -70v. Capacitors C443 and C444 have been added to prevent hunting. Resistors R442 and R443 are included to limit the peak current to transistor Q441 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q441. Resistor R444 provides a path for the leakage current of Q442 so that this current does not affect the base current in Q441. This allows Q441 to be more nearly cut off during a light load. This -65v power supply is stacked on the bottom of the -20v supply giving a combined output of -85v.



Schematic
165-4C Power Supply
Dwg. #D16554C



NOTES:
1. ALL WIRE 22GA. UNLESS SPECIFIED.
2. ALL A.C. WIRES TO BE TWISTED IN PAIRS.

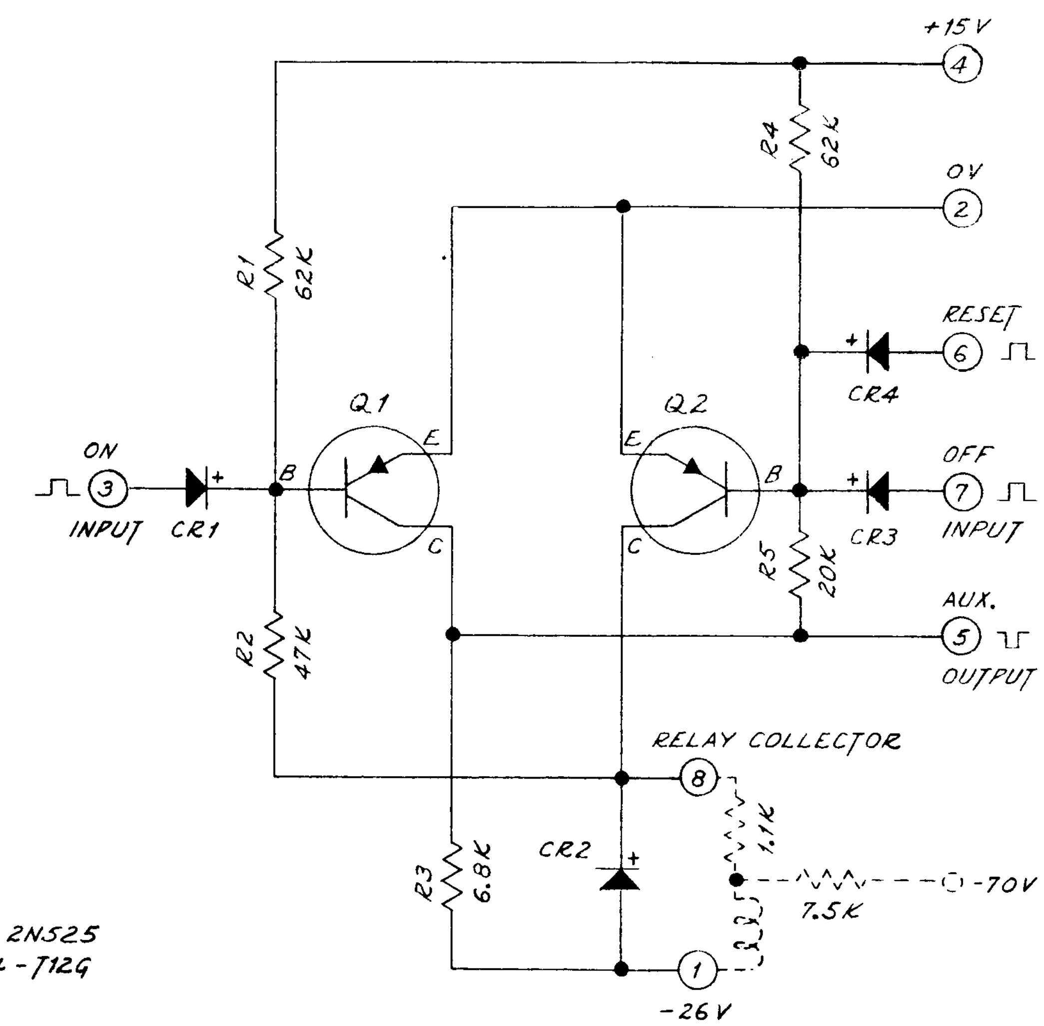
P401

PIN	DEST.	FUNCTION	WIRE	PIN	DEST	FUNCTION	WIRE
1	T401-1	AC INPUT	(W) 20	41			
2	T401-1	AC INPUT	(W) 20	42			
3				43			
4	F404	AC INPUT	(BR) 20	44	F401	+12 V	(W-R) 20
5	F404	AC INPUT	(BR) 20	45	TB401-25	0 V	(BK) 20
6				46	TB401-25	0 V	(BK) 20
7				47	F402	-20 V	(W-S) 20
8				48	F402	-20 V	(W-S) 20
[illegible]	TP-[illegible]	[illegible]	(Y) 20	49	[illegible]	[illegible]	(W) 20
[illegible]	[illegible]	[illegible]	[illegible] 20	50	[illegible]	CHASSIS GND	(BK)

Wiring Diagram
165-4C Power Supply
Dwg. #E165W46

TN 28
RELAY DRIVING FLIP-FLOP

A TN28 is a bistable flip-flop which can be used for driving a relay coil or other loads of 500 ohms or more. The external load (shown on the schematic diagram in phantom between pins 8 and 1) is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" or "0" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "on" or "1" condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize. Assuming that Q1 is saturated, then its collector is approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -.05 volts; so the current through resistor R1 is approximately 0.25 milliamps. The current through the series combination of R2 and the external load resistor, which may very from 500 ohms to 5K, varies from 0.53 to 0.48 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so this condition is a stable one. The input voltages at pins 3, 6 and 7 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Now resistors R1 and R2 are connected from +15 to 0 volts and hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This, then, is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR2 is included to suppress the voltage of an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cutoff, the relay coil is de-energized. However, the inductance of the relay coil attempts to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and so does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil and eliminating the voltage spike. Although the description of operation of this network has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.



Q1, Q2 - 2N525
CR1-CR4 - T12G

Schematic,

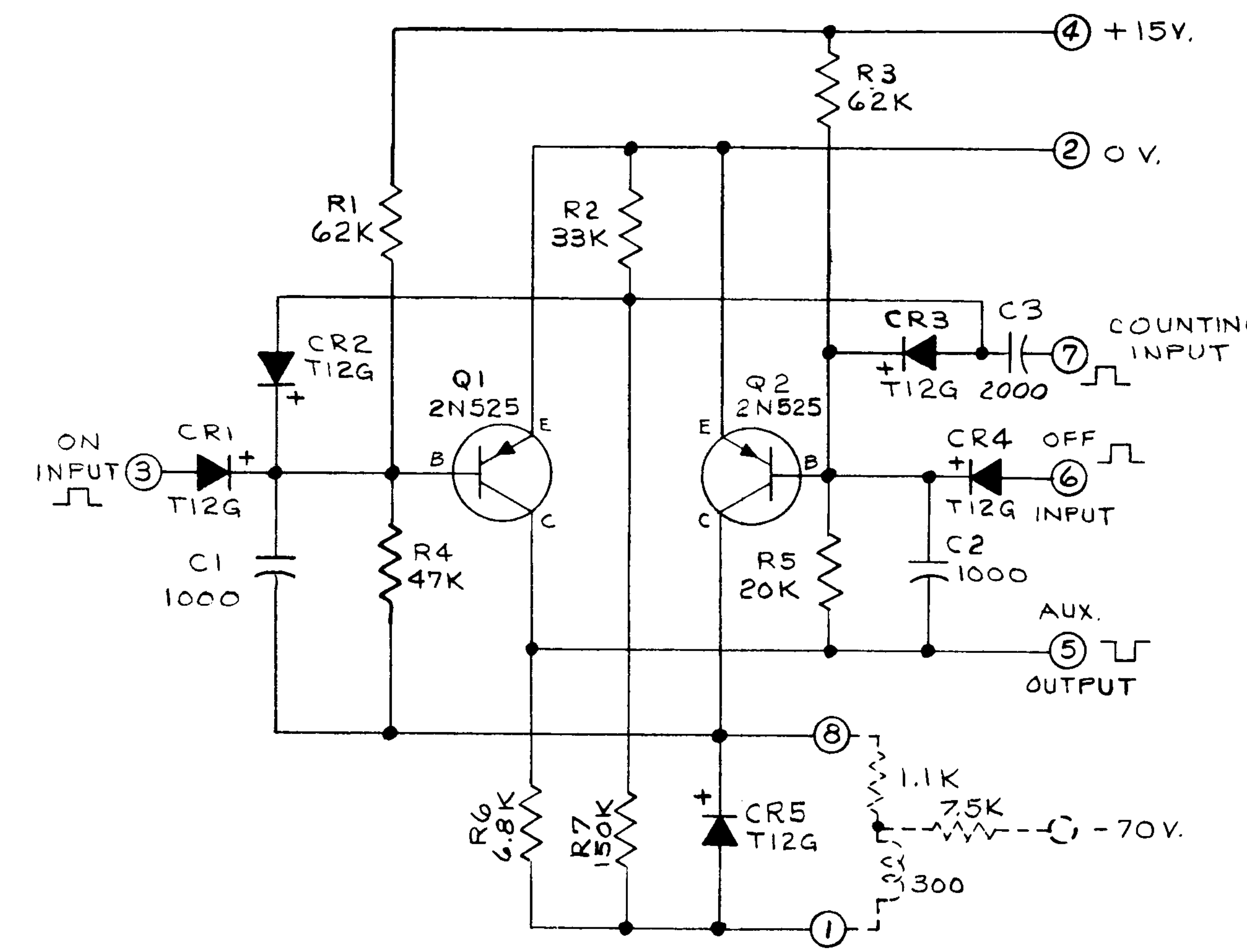
TN28 Relay Driving Flip-Flop

Dwg. #A103S28A

TN 42
RELAY DRIVING COUNTING FLIP-FLOP

TN42 is a counting type bistable flip-flop which can be used to drive a relay coil or other loads 500 ohms or more. The external load which is shown on the schematic diagram as dotted between pins 8 and 1 is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" condition when transistor Q1 is saturated and Q2 is cut off leaving the relay de-energized. The "on" or "1" condition is in the opposite, with Q1 cut off and Q2 saturated causing the relay to energize. If we assume that Q1 is saturated then its collector will be at approximately -0.25 volts. Resistors R3 and R5 are then connected from +15 to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias will keep Q2 cut off. With Q1 saturated its base will be at approximately -0.5 volts so the current through resistor R1 is 0.25 ma. The current through the series combination of R4 and the external load resistor, which may vary from 500 ohms to 5K, will vary from 0.53 to 0.48 ma. The difference between the current in R1 and the current in R4 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so that condition is a stable one. The input voltages at pins 3 and 6 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 will conduct, raising the base voltage of Q1 to a positive value. It should be noted that the input pulse will be loaded somewhat so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off R3 and R5 are no longer connected between 0 volts and +15 volts and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R6 causing Q2 to saturate. Now resistors R1 and R4 will be connected from +15 to 0 volts and will hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This then is the other stable condition, which will be maintained until Q2 is cut off by a positive pulse at pin 6. A positive pulse at pin 6 will turn Q2 off, allowing the base current from Q1 to be conducted through R4 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR5 is included to suppress an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cut off the relay coil is de-energized. However, the inductance of the relay coil will attempt to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR5 is added. During most phases of the cycle CR5 will be reverse biased and therefore will not enter into the operation of the circuit. But when the relay is de-energized and pin 8 is driven negative by the relay inductance, CR5 is now forward biased and conducts, providing a path for current through the relay coil and eliminating the voltage spike.

The actions just described cover the operation of this network as a conventional bi-stable flip-flop which requires a turn-on pulse and a turn-off pulse. In addition, this network can be used for counting by using the pin 7 input. R2 and R7 act as a divider network which establishes their junction at -4.5 volts. Since the bases of Q1 and Q2 are either at -0.5 volts or at a positive voltage, both CR2 and CR3 will normally be reverse biased and non-conducting. By applying a positive pulse approximately 10 volts high with a rise time of approximately 0.5 microseconds to pin 7, the junction of R2 and R7 will be raised to +5.5 volts until C3 discharges. This will permit both CR2 and CR3 to conduct, which will cut off both Q1 and Q2 simultaneously. Assume the condition before the input pulse was Q1 saturated and Q2 cut off. When both are cut off by the input pulse there will be no drop in voltage at the collector of Q2, hence no pulse coupled through C1. But when Q1 cuts off the resulting drop in voltage at the Q1 collector is coupled through C2 to the base of Q2. The result is that when the input pulse has been differentiated (C3 charges up) and no longer has an effect, C2 forces Q2 to conduct. When the next positive pulse is applied to pin 7, the resulting drop in voltage at the Q2 collector will force Q1 to turn on first. In this way the state of the network will change from a "0" to a "1" or reverse for every positive pulse that is applied to pin 7.



Schematic,

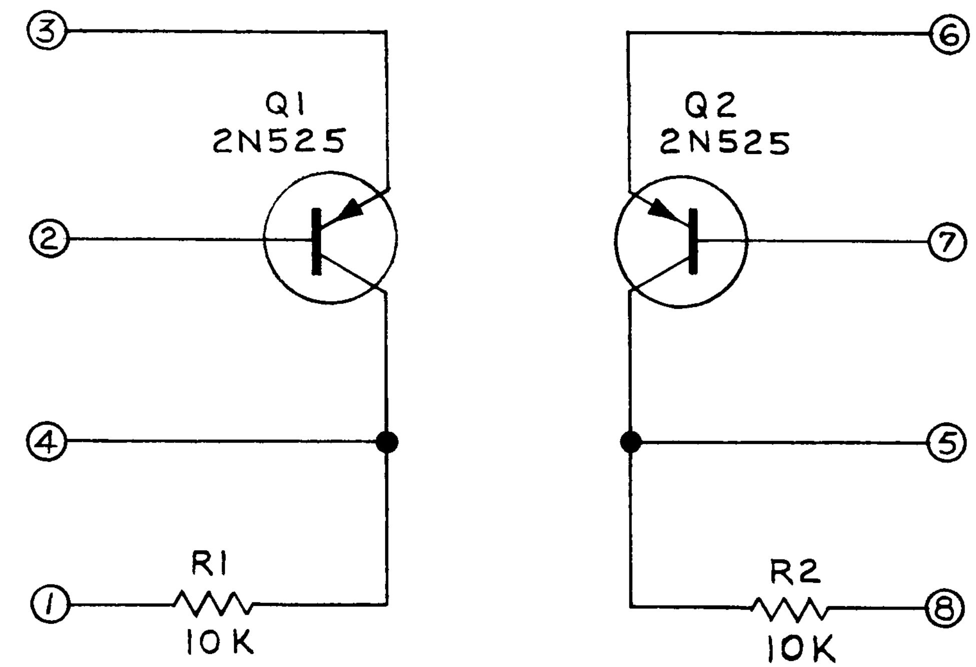
TN42 Relay Driving Counting Flip-Flop

Dwg. #A103S42A

TN 57
DUAL PULSE AMPLIFIER

The TN57 contains two PNP transistors connected as two independent conventional amplifiers. Only one of these will be discussed since the other is identical to it. As normally used, a supply voltage is connected to pins 3 and 1 with the plus side on pin 3. Pin 2 will be the input and pin 4 the output. As long as pin 2 is more positive than pin 3 the transistor is cut off and the voltage at pin 4 will be the same as the voltage at pin 1. When pin 2 is approximately 0.5 volts negative with respect to pin 3 the transistor will saturate and the voltage at pin 4 will go positive until it saturates, approximately 0.25 volts more negative than the emitter. Caution must be used to connect an external base resistor in series with pin 3 to prevent damage to the transistor. The value of the external base resistor is dependent upon how negative the driving voltage goes and upon the external load that is connected to pin 4. To insure saturation the base current should be at least 1/20th of the collector current.

The TN57 may also be used in a variety of applications by the addition of external components.

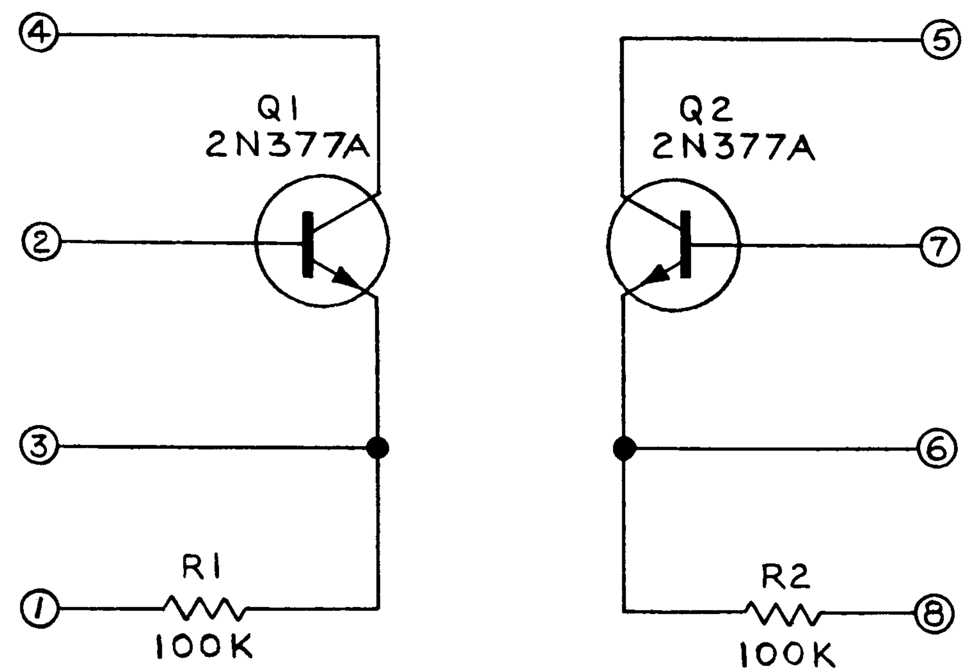


Schematic
TN57 Dual Pulse Amplifier
Dwg. #A103S57A

TN 58
DUAL EMITTER FOLLOWER

A TN58 consists of two NPN transistors connected as independent emitter followers. As normally used, a supply voltage is connected to pins 4 and 1 with the plus side on pin 4. As the voltage at pin 2 is varied, between the voltages at pins 4 and 1, the transistor will conduct and the voltage at the emitter, pin 3, will be approximately 0.4 volts more negative than the voltage at pin 2. Because of the power gain of the transistor a lower impedance load can be driven from pin 3 than could have been driven from the signal applied to pin 2.

The TN58 may also be used in a variety of applications by the addition of external components.

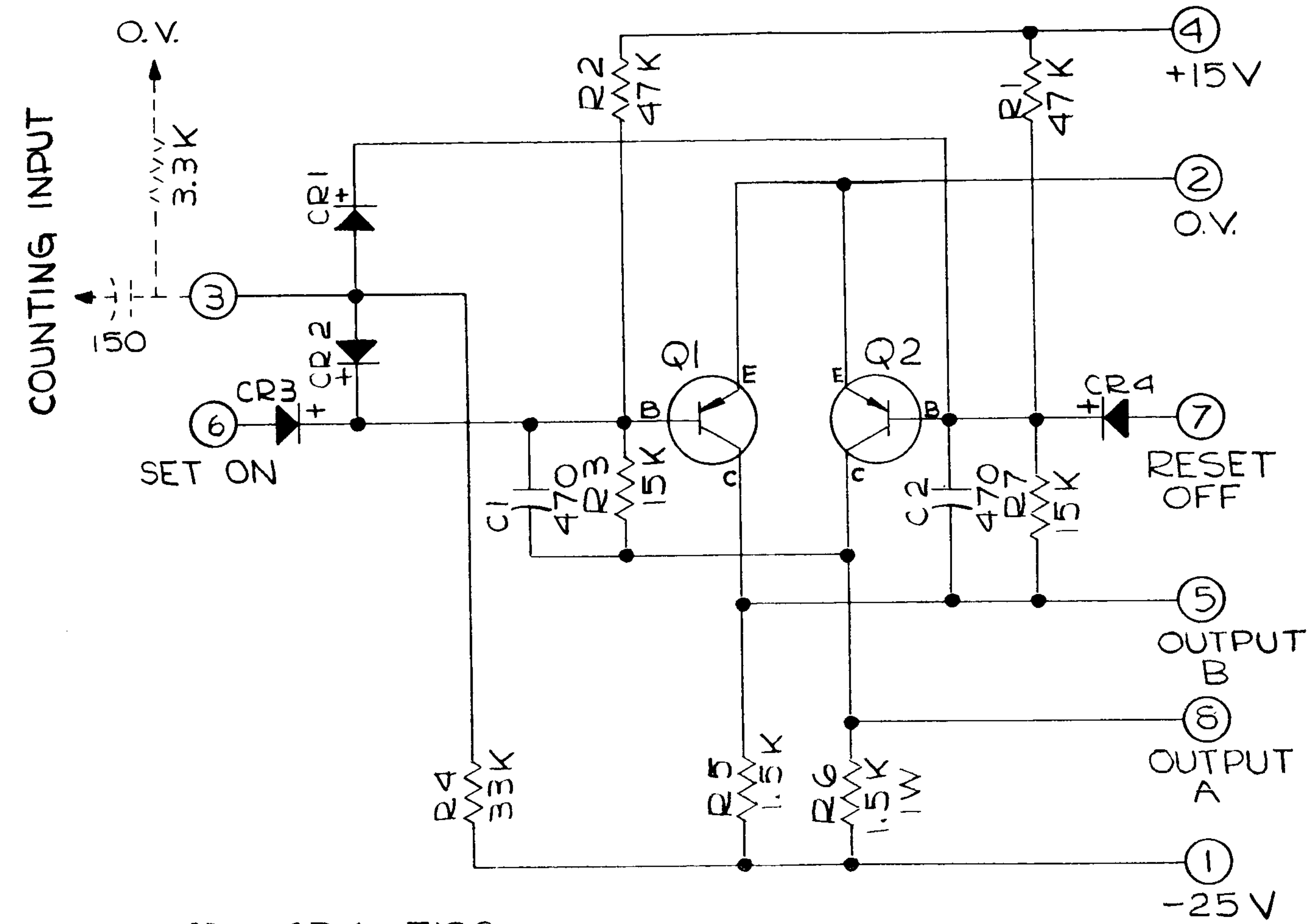


Schematic
TN58 Dual Emitter Follower
Dwg. #A103S58A

TN 90 B
BALANCED FLIP-FLOP AND DIVIDER

The TN90B is a bistable balanced flip-flop. An auxiliary input (pin 3) allows the network to be used as a divider in a counter.

The network is defined as being in the "0" state when Q1 is saturated and Q2 is off and in the "1" state when the reverse is true. Assume that Q1 is saturated ("0" state) then the collector voltage of Q1 will be approximately 0 volts and resistor divider, R1 and R7, will maintain approximately +3.5 volts of reverse bias on the base of Q2, keeping it cut off. With Q2 cut off, resistors R3 and R6 will provide a path for Q1 base current, clamping Q1 in saturation. This condition is stable and will not be changed until an input is received on pin 3 or pin 6. Pin 6 is in the "1" input, in that a positive pulse above 0volts pin 6 will cause CR3 to conduct, thus drive the base of Q1 positive above 0volts, reverse biasing Q1, subsequently cutting Q1 off. As Q1 is cut off its collector will go negative and due to the resistor divider, R1 and R7, the base of Q2 will go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and due to the resistor divider of R2 and R3 the base of Q1 will be reverse biased at approximately +3.5 volts, keepingQ1 cut off, after the input pulse has passed. The network will remain in the "1" state until reset by a positive pulse on pin 7 or triggered from a pulse on pin 3, the counting input. If a positive pulse is applied on pin 3 through an external capacitor for differentiation, both Q1 and Q2 will be cut off. Capacitors C1 and C2 retain charges which are dependent upon which one of the transistors was saturated before the input pulse occured. Since the input pulse is differentiated by a small input capacitor, it will last a very short time, less than one microsecond. At this point, the internal capacitors C1 and C2 take over, turning on the transistor that had previously been off. For example; assume the network is the "1"state, therefore Q1 is cut off and Q2 is saturated. The voltage across C1 will be approximately 3.5 volts and across C2 will be approximately 26 volts. When pin 3 goes positive above 0 volts, both bases will be driven positive, cutting the transistors off. The collector of Q2 starts to go negative from 0volts to -23volts. Since this occurs almost instantaneously and C1 has been charged only 3.5 volts the base of Q1 will go negative, turning Q1 on. As Q1 is turned on, Q2 is held cut off and we are now in the "0" state as explained previously. Npte, since the collector of Q1 was at -23 volts before the pulse occurred on pin 3 and there wasn't any change of collector voltage when the pulse did occur. The base of Q2 would not experience any change through C2. The output pins of the network are 5 and 8. When the network is in the "0" state pin 5 will be at 0volts and pin 8 will be approximately -23 volts and the reverse is true when the network is in the "1" state. Although the description of operation has been based on voltages of +15 volts and -25 volts this network will operate equally on voltages of +12volts and -20volts or +10volts and -15volts.



CR1 - CR4 - T12G
Q1 & Q2 - 2N316

Schematic,

TN90B Balanced Flip-Flop and Divider

Dwg. #A 103S90B

TN 130 B
CORE DRIVER

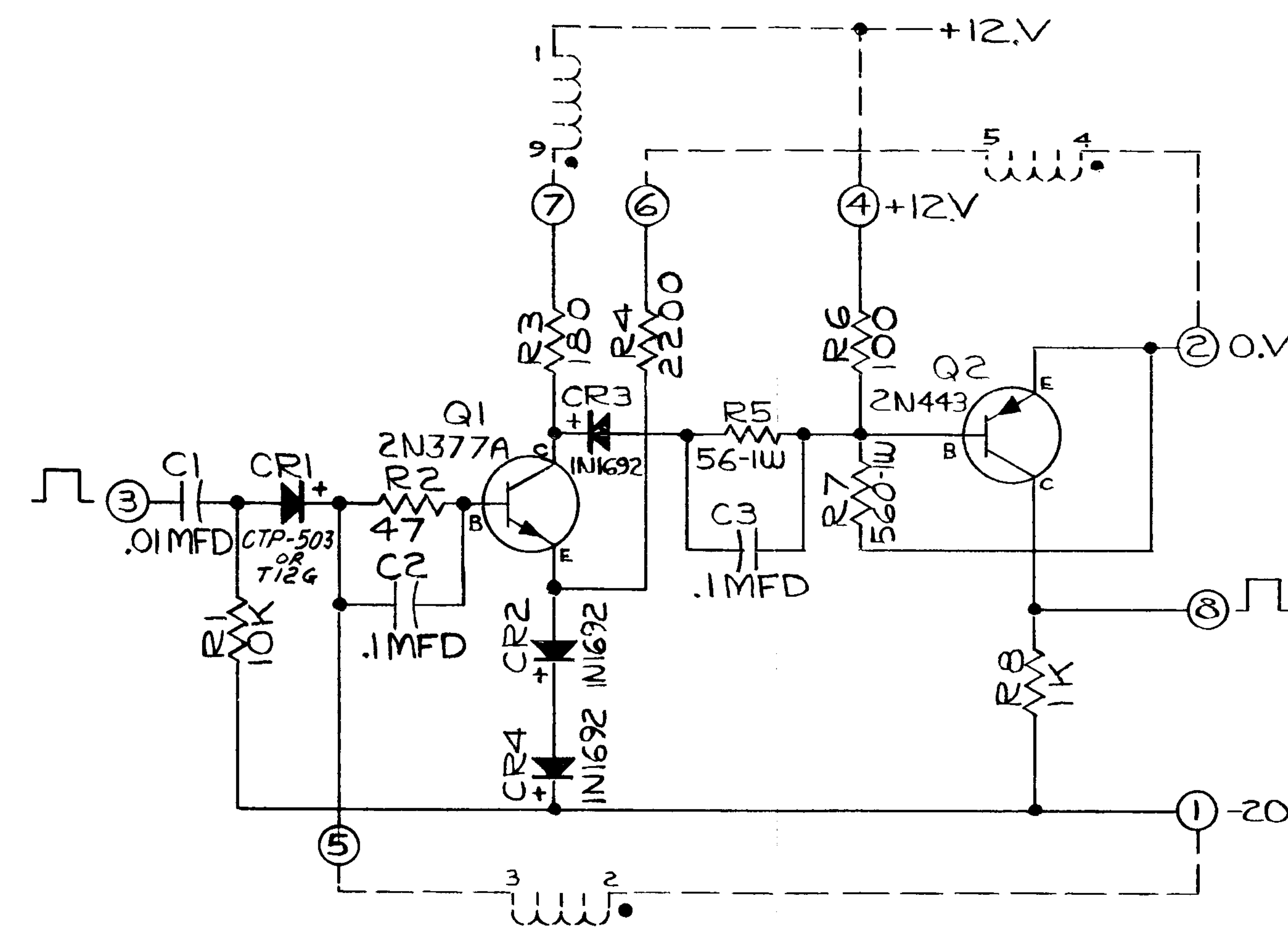
The TN130B is a blocking oscillator with amplifier which generates a positive going pulse from -20 volts to 0 volts, with a time duration determined by the core with which it is used. The TN130B is normally used with a MEC Model MN13 core, which gives it a pulse width of approximately 40 microseconds.

In the quiescent condition, transistor Q1 is maintained in cut off. The emitter voltage of Q1 is determined by the forward voltage drop of diodes CR2 and CR4 (1.5 volts) and is at approximately -18.5 volts. The base of Q1 is returned to -20 volts through R2 and the feedback winding of the core, connected from pin 5 to -20 volts. The d-c impedance of the feedback winding is approximately 5 ohms; thus the base of Q1 is nearly -20 volts, keeping Q1 reverse biased approximately 0.7 volts and properly cut off. Since there is no Q1 collector current, the collector voltage is +12 volts.

A positive going input pulse at pin 3 is coupled by capacitor C1, diode CR1, and capacitor C2, paralleled with R2 to the base of Q1. This pulse starts Q1 conducting. The resulting Q1 collector current passes through the collector winding of the external core. This generates a voltage across the collector winding coupled through the core to the feedback winding. By noting the phasing of the windings on the core, it can be seen that, as the collector voltage becomes negative, the voltage at pin 5 is becoming positive. This in turn drives Q1 further into conduction, even after the input pulse has been differentiated by C1. Q1 saturates in approximately one microsecond with an emitter-collector voltage of approximately 0.25 volts. Q1 will remain saturated as long as transformer action in the core continues to drive pin 5 of the TN network sufficiently positive to cause Q1 base current to flow. The pulse width (approximately 40 microseconds for an MN13 core) is determined by the characteristics of the core.

When the core material finally reaches saturation, transformer action in the core will cease, the feedback winding will no longer drive pin 5 positive, and Q1 base current will stop. This cuts off Q1. With no current in the collector winding of the core, the current in the reset winding resets the core. This reset current is furnished to the reset winding (pins 4 and 5 of the core) through resistor R4 and diodes CR2 and CR4. This involves going from the plus saturation condition attained during the output pulse to a minus saturation condition (reset). During this time, the voltages at the feedback winding and the collector winding are reversed. The reversal of a voltage at the feedback winding increases the reverse bias on Q1. The reversal of voltage in the collector winding tends to drive the output voltage somewhat more positive than the +12 volts on pin 7. It takes approximately 30 microseconds for the reset action to be accomplished.

The amplifier section Q2 is normally biased to cutoff by voltage divider R7 and R6. With no collector current flowing, the quiescent collector voltage of Q2 is -20 volts. The negative going pulse generated by the blocking oscillator section is coupled to the amplifier base through CR3, R5, and C3. The diode provides for rapid cut off of the amplifier, thereby minimizing the fall time. R5 and C3 serve as base current limiting and rise time determinants. The load is connected between -20 volts and 0 volts and should be limited to no less than 8 ohms (20 to 24 MN11 cores).



NOTE:
ALL RESISTORS ½ WATT ±10%
UNLESS OTHERWISE NOTED.

Schematic,

TN130B Core Driver

Dwg. #A103S130B

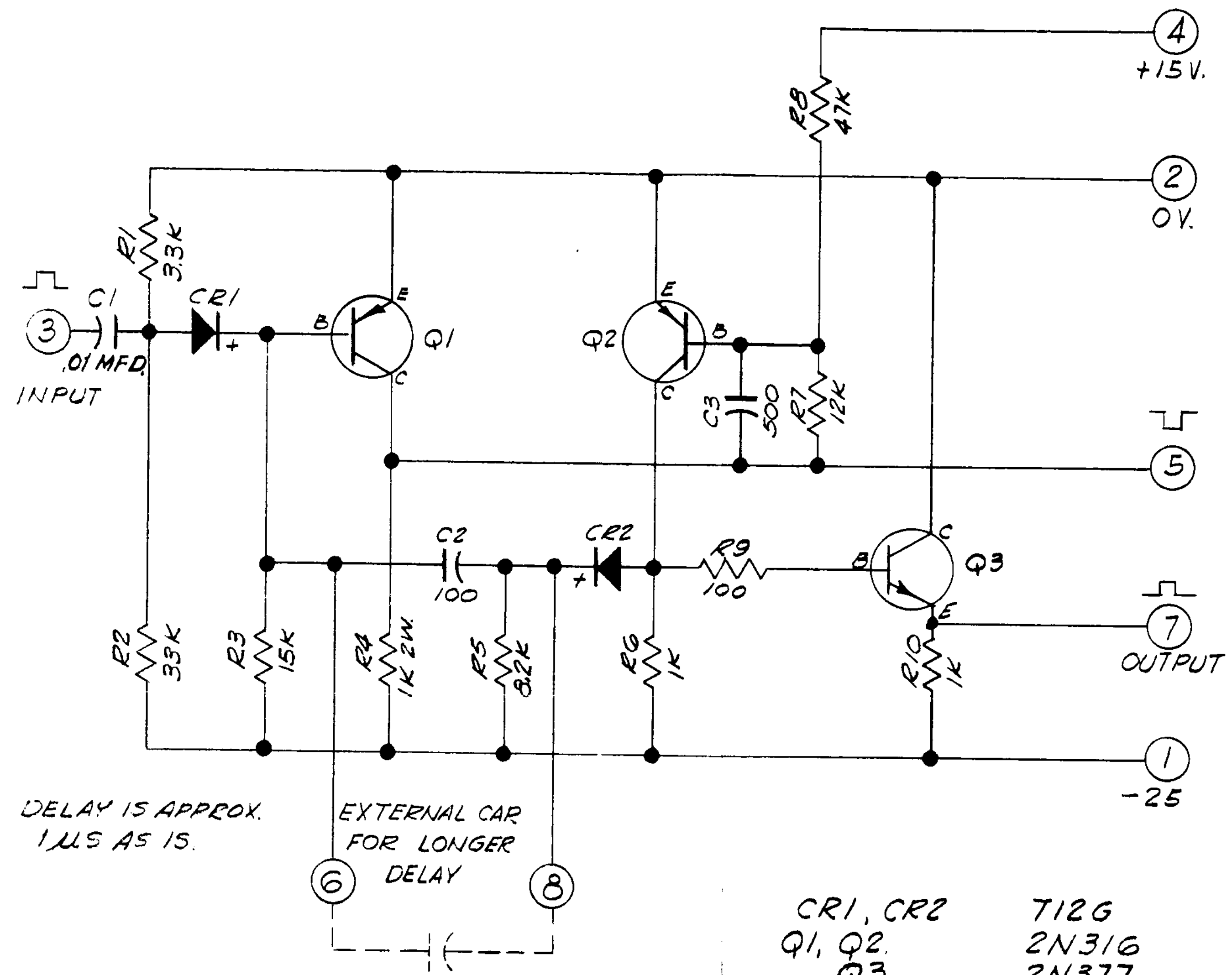
TN 138
ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138 is a monostable flip-flop used for generating a pulse which can be varied in width from a minimum of about 2 microseconds to over 200 microseconds. In quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage dividers R7 and R8 are connected between +15 volts and 0 volts, establishing a positive bias voltage on the Q2 base, and keeping Q2 cut off. Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise does not trigger the network.

A positive pulse of not less than 10 volts, with a rise time not greater than 1 microsecond, will trigger the network by cutting off transistor Q1. Q1 is cut off when the input pulse raises the base voltage above 0 volts. Capacitor C1 is used to differentiate the input pulse so that a long duration pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts to nearly 0 volts. This rise of voltage is coupled to the base of transistor Q1 through capacitor C2, keeping transistor Q1 at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return to less than 0 volts. Q1 now saturates again and cuts off Q2. This time can be lengthened by adding capacitance in parallel with capacitor C2.

The terminals of C2 are brought out on pins 6 and 8 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a d-c path for current of C2. Q3 is the emitter-follower which will drive a load of 200 ohms.

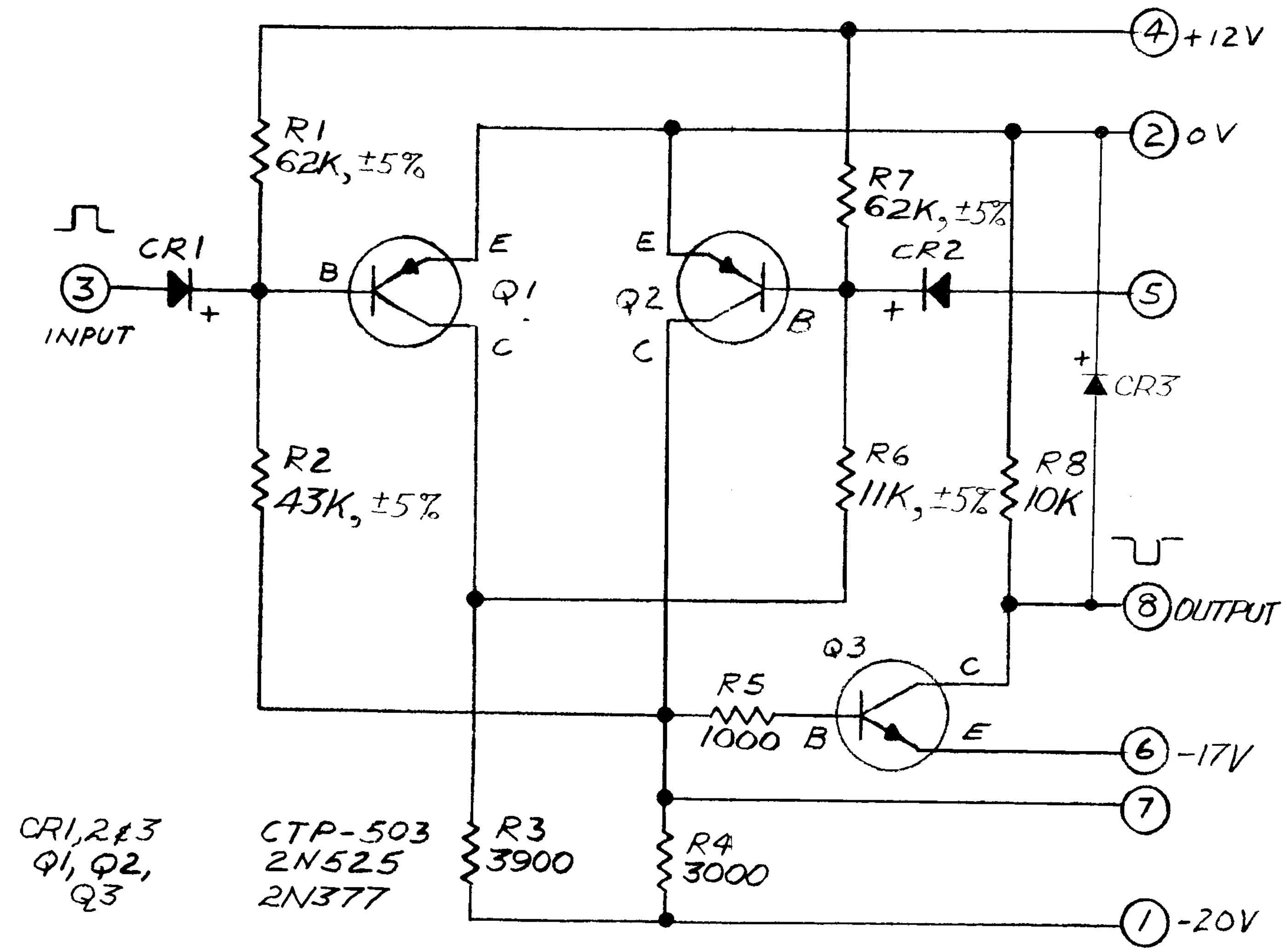


CR1, CR2 T12G
Q1, Q2. 2N316
Q3 2N377

Schematic
TN138
Dwg. #A103S138

TN 144
FLIP-FLOP WITH PULSE AMPLIFIER OUTPUT

A TN144 is a bistable flip-flop with a pulse amplifier output which can be used to drive a load of 85 ohms or more. Since most flip-flops are limited to the amount of loading, which affects the switching of the flip-flop, a pulse amplifier has been added to permit greater loads. A transistorized neon indicator may be connected in parallel with the load to indicate the states of the flip-flop. The network is normally defined as being in the "0" state when transistor Q1 is saturated and Q2 and Q3 are cut off. The "1" state is the condition when Q1 is cut off and Q2 and Q3 are saturated. Assuming that Q1 is saturated ("0" state), then its collector is at approximately -0.25 volt. Resistors R7 and R6 are then connected from +12 volts to 0 volts, and by divider action hold the base of Q2 at approximately +1.8 volts. Since the emitter of Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -0.5 volt, so the current through resistor R1 is approximately 0.2 milliamps. Since Q2 is cut off, its collector is at approximately -19 volts, and the current through R2 and R4 is therefore 0.4 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to clamp Q1 in saturation. This mode of operation is therefore stable. Q3 is cut off when Q2 is cut off, since the base of Q3 is at -19 volts, reverse biasing the emitter. Since Q3 is cut off, there is no collector current (except for leakage) and pin 8 is at approximately 0 volts. The input voltages at pins 3 and 5 must be somewhat negative during quiescent conditions. The flip-flop may be triggered to the "1" state by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, thus raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cuts off. With Q1 cut off, R7 and R6 are no longer connected between the +12 volts and 0 volts, and Q2 is no longer clamped off. Instead, base current of Q2 may now flow through resistors R6 and R3, cuasing Q2 to saturate. Now resistors R1 and R2 are connected from +12 volts to 0 volts, and clamp the base of Q1 at approximately +5 volts, holding Q1 in a cut off condition after the input pulse passes. As Q2 is saturated and its collector goes positive, the base of Q3 goes positive enough to allow Q3 to saturate. R5 limits the base current of Q3. As Q3 saturates, pin 8 (the output pin) goes negative to approximately -17 volts. R8 is the collector load resistor of Q3, to furnish a minimum collector current when there is no external load from pin 8 of the network to 0 volts. This is the other stable condition which will be maintained until Q2 is cut off by a positive pulse on pin 5. A positive pulse (normally called reset) on pin 5 will allow base current from Q1 to be conducted through R2 and R4, driving Q1 back into saturation and restoring the initial condition. Diode CR3 is included to suppress the inductive effects of an external relay coil (if used) connected across pins 8 and 2. As Q3 goes from saturation to cut off, the relay coil is de-energized. However, the inductance of the relay coil attempts to maintain the current through it by driving the voltage at pin 8 much more positive than 0 volts. If this were allowed to happen, Q2 could be damaged by the excessive collector-emitter voltage. During most phases of the cycle, CR3 is reverse biased; consequently, it does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven positive by the relay inductance, CR3 is forward biased and conducts, providing a path for the current through the relay coil and eliminating the excessive transient voltage to appear on the collector of Q3.



Schematic,

TN144 Flip-Flop with Pulse Amplifier Output

Dwg. #A103S144A

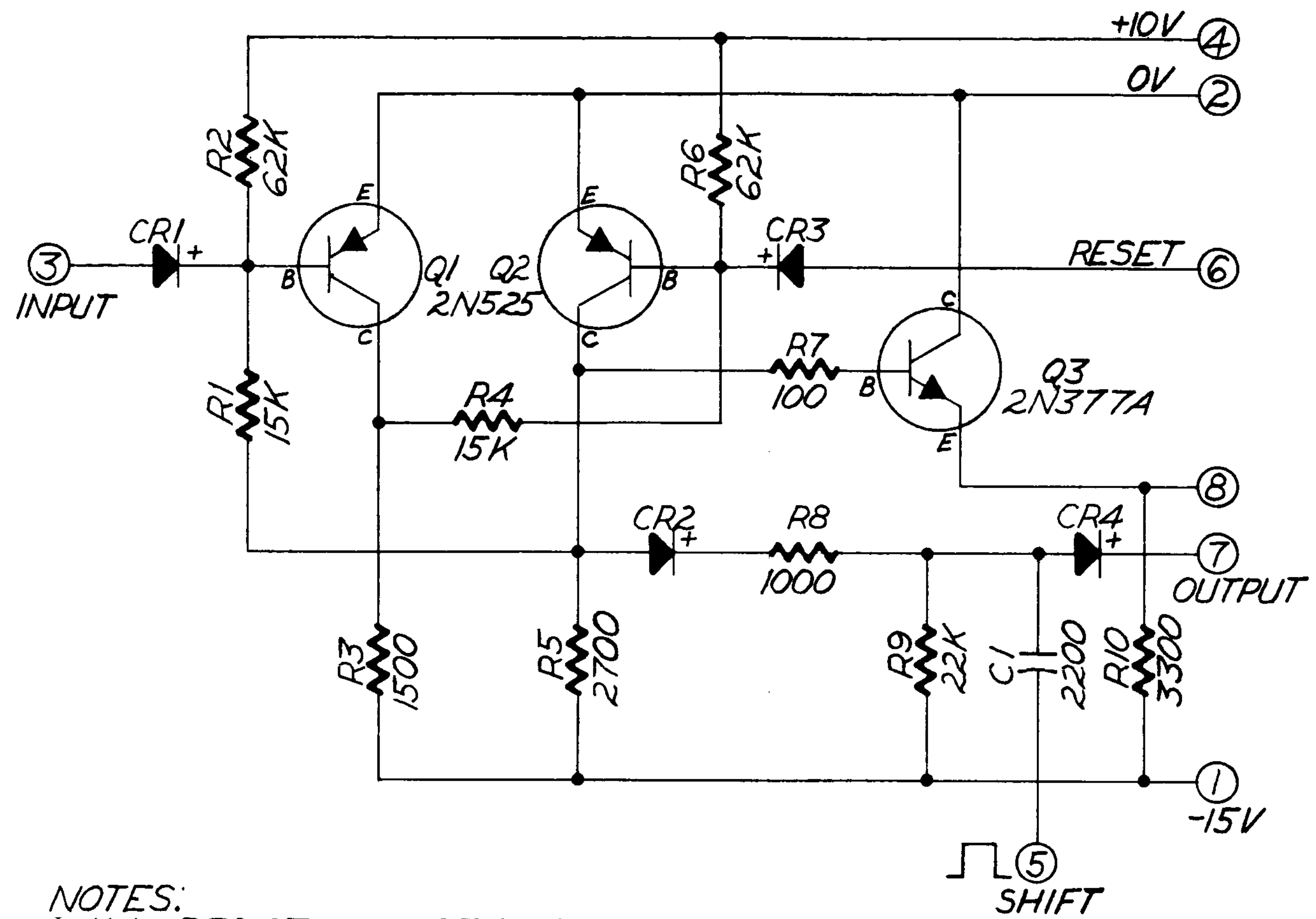
TN 154
SHIFT REGISTER FLIP-FLOP WITH EMITTER FOLLOWER OUTPUT

The TN154 is a bi-stable flip-flop normally used in a shift register which has an internal shift network and an emitter follower as an output. The internal shift network is used as the shift register serial output; that is, pin 7 of one TN154 is directly coupled to pin 3 of the next TN154. The emitter follower output, pin 8, is used to read out data in parallel from the shift registers. A transistorized neon light is normally connected, in parallel with the load, to pin 8, to indicate the states of the flip-flops. The light is lit when the network is in the "1" state, and off when the network is in the "0" state.

The "0" state is defined as the condition when Q1 is saturated and Q2 and Q3 are cut off. The "1" state is the condition in which the reverse is true. Assume Q1 is saturated ("0" state); then the collector voltage of Q1 will be approximately 0 volts, and the resistor divider of R4 and R6 will maintain +2 volts on the base of Q2. This will constitute a reverse bias on Q2, keeping it cut off. With Q2 cut off, resistors R1 and R5 will provide a path for Q1 base current, clamping Q1 in saturation. Since Q2 is cut off, its collector will be at approximately -13 volts; therefore the base of Q3 will be at -13 volts. This will keep Q3 near cut off, and the data output, (pin 8), will be at -13 volts. This condition is stable and will not be changed until a positive pulse above 0 volts on pin 3 causes CR1 to conduct. When CR1 conducts, the base of Q1 is driven positive above 0 volts, reverse biasing Q1, and subsequently cutting H off. As Q1 is cut off, its collector will go negative; due to the resistor divider, R4 and R6, the base of Q2 will also go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and, due to the resistor dividers R1 and R2, the base of Q1 will be clamped at approximately +2 volts. This keeps Q1 cut off after the input pulse has passed. Also at this time the base of Q3 will go positive, like the collector of Q2, and Q3 will saturate. Therefore the emitter of Q3 and pin 8 will go to 0 volts. The network is now in the "1" state and will remain there until reset by a positive pulse above 0 volts on pin 6. When this does occur, the network will go to the "0" state as described previously and pin 8 will go to -13 volts.

When Q2 is conducting, (a pulse has occurred on pin 3), capacitor C1 charges through CR2 and R8. CR2 is used to prevent the shift pulse from back triggering the flip-flop and to keep the charge on C1 from leaking off rapidly through R5. When shifting information through the register, the shift input, (pin 5) goes from -10 volts to approximately 0 volts for 5 microseconds. If the TN is in the "0" state, the junction of C1 and CR4 will go from -14 volts to -4 volts and back to -14 volts. If the TN is in the "1" state, this junction will move from -2 volts to +8 volts and back to -2 volts. In a shift register, pin 7 of one TN154 is connected to pin 3 of the next TN154. The pulse at the junction of C1 and CR4 will have no effect on the next flip-flop unless it goes above 0 volts. This will occur only if a "1" (Q2 saturated) is present in the first network. The reset pulse is necessary in order to reset all the TN's to a "0" state before the shift pulse, since transmitting a "1" or "0" to the next stage does not automatically remove a "1" from the preceding stage. In shifting, the 5 microsecond reset pulse first triggers all the TN's to the "0" state, and then the 5 microsecond shift pulse advances the "1" that has been temporarily stored in the capacitor. Capacitor C1 starts to discharge when the reset pulse cuts off Q2, but the RC time constant of C2 and R9 is long enough so that it will *not* discharge significantly before the shift pulse occurs. CR2 will be charged 10 volts by the shift pulse. If the junction was at -2 volts ("1" state) before reset, the shift pulse will cause the junction to rise from -2 volts to +8 volts. CR6 will conduct, causing pin 5 of the next network to go positive, thus inserting a "1". If the junction was at -14 volts ("0" state) before reset, then this junction will rise to -4 volts when the shift pulse occurs, and CR6 will not conduct, because it is reverse biased. Therefore the next network will remain in the "0" state, and a "0" has been shifted.

Q3 is an emitter follower to isolate the flip-flop so that a lower impedence load can be driven from the parallel output of a shift register.



NOTES:
1. ALL RESISTORS ARE ±10%, 1/2 W UNLESS NOTED.
2. ALL DIODES ARE CTP-503 UNLESS NOTED.

Schematic
TN154
Dwg. # 103S154A

TN 158
CONTROLLED ONE-SHOT

The TN-158 is a controlled one-shot (mono-stable multivibrator) with an emitter follower output. It is controlled, because the unstable state may be terminated at any time by an input pulse on pin 5. This network can drive low impedance loads because of the emitter follower output.

The network's quiescent state is with Q1 saturated, and with Q2 cut off. The base of Q1 is forward biased by R3, which is connected to -20 volts, saturating Q1. Since Q1 is saturated, the base of Q2 is reverse-biased by voltage divider R6 and R7 between +12 volts and the collector of Q1 (0 volts). With Q1 saturated, its collector is at approximately 0 volts; therefore, the base of Q3 is at the same voltage, forward biasing Q3 and keeping it saturated. Therefore, pin 7 will be at approximately 0 volts. The resistor divider of R1 and R2 will maintain a reverse bias on diode CR1 of approximately 2 volts.

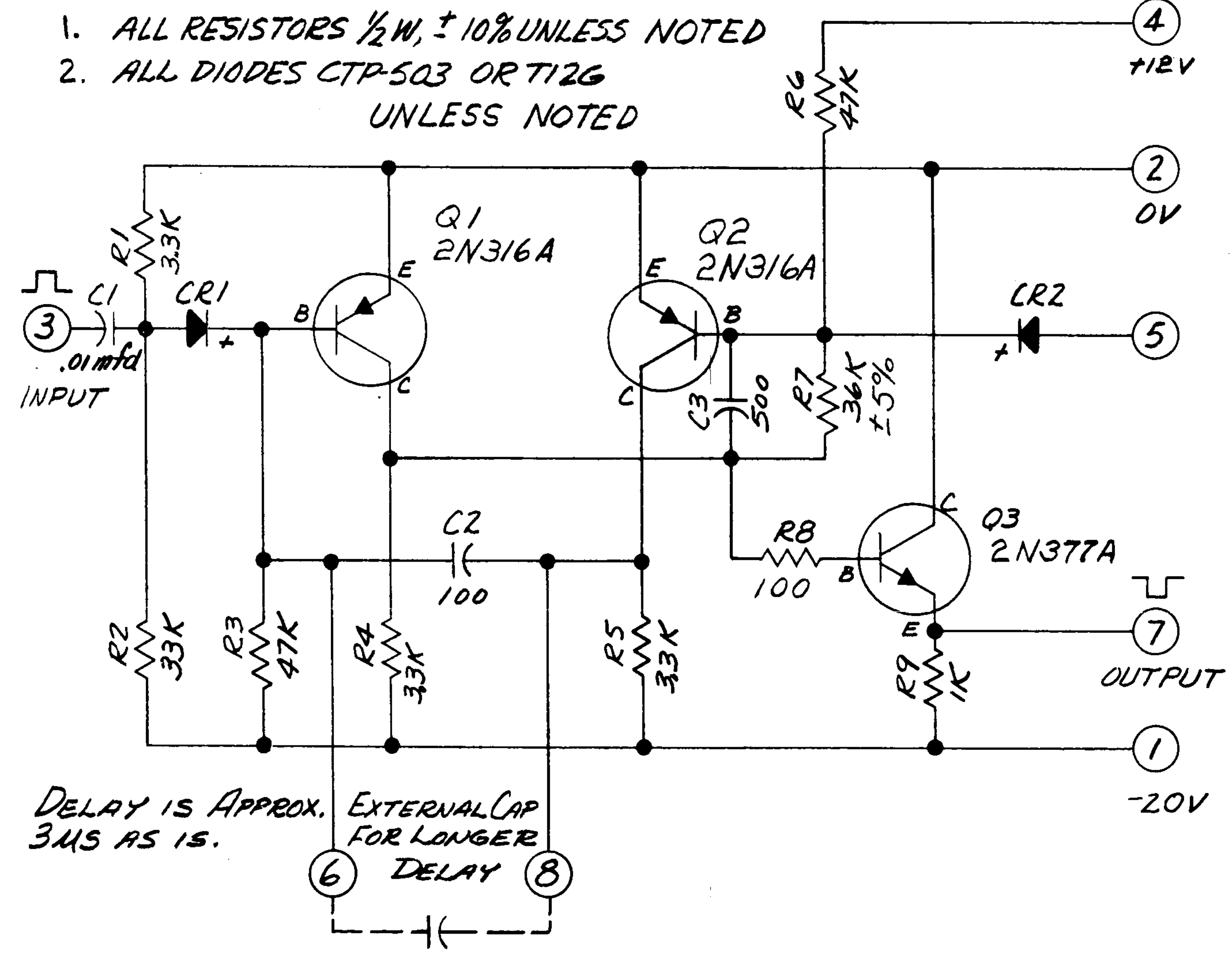
Now, when a positive pulse of sufficient amplitude is applied to pin 3 to cause conduction of CR1, transistor Q1 will be cut off. The collector of Q1 will therefore go negative toward -20 volts. This negative going potential is coupled to the base of Q2 through C3 and R7. This will cause the base of Q2 to go negative with respect to the emitter. Q2 will conduct, and starts to saturate rapidly. The collector of Q2 will now go positive (from -20 volts to 0 volts), and this voltage change, coupled through C2 to the base of Q1, will keep Q1 cut off after the input pulse has passed. When Q1 is cut off, Q3 will also be cut off, and pin 7 will go to -20 volts. C2 has now been charged, and will start to discharge through R3. When C2 has discharged sufficiently to allow the base of Q1 to return to its quiescent negative potential, Q1 will saturate. As Q1 saturates, its collector will go positive, and, due to the resistor divider R6 and R7, the base of Q2 will go positive. This reverse biases Q2, cutting it off. When Q1 is saturated, the base of Q3 will be positive with respect to the emitter, and this will cause Q3 to go into saturation. Pin 7, the output of the emitter follower, will return to 0 volts. The one-shot has now returned to its quiescent condition.

The time constant for R3 and C2 determines the pulse width, or the time duration of the unstable state, which is about 3 microseconds. By adding external capacity across pins 6 and 8, the RC time constant is increased, and thus the pulse width is increased. Pin 5 is an auxiliary input, and is used to shorten the existing time duration of the unstable state. That is, a positive pulse on pin 5 will cause Q2 to be cut off before the normal RC time of the circuit.

Assuming that the network is in the unstable state: Q1 is cut off and Q2 is saturated, while C2 is starting to discharge. A positive pulse, above 0 volts occurs on pin 5, causing CR2 to conduct. The base of Q2 will be reverse-biased, therefore Q2 will be cut off. As Q2 is cut off, its collector will go negative toward -20 volts. This negative going potential is coupled to the base of Q1 through C2. This will cause Q1 to be forward-biased, and it will start to saturate. Q2 will be held cut off by the same divider as explained previously. By cutting off Q2 from a pulse on pin 5, we have caused C2 to discharge rapidly; therefore, the one-shot is returned to its stable or quiescent state immediately.

Although the description of operation has been based on voltages of +12 volts and -20 volts, this network will operate equally as well on voltages of +10v and -15v.

NOTES:
1. ALL RESISTORS ½W, ± 10% UNLESS NOTED
2. ALL DIODES CTP-503 OR T12G UNLESS NOTED



DELAY IS APPROX. 3µS AS IS.

EXTERNAL CAP FOR LONGER DELAY

MAGNETIC CORES

1. GENERAL

A component commonly used in digital data handling equipment is a magnetic core. The term magnetic core is usually applied to a small torroid composed of magnetic material which has high permeability and also high retention. This material will have what is called a square hysteresis loop, shown in Point A, Figure MN-1. Because of this square hysteresis loop, there are two stable energy states, which make the cores adaptable to digital circuits. Magnetic cores are commonly used for shift registers, "and" gates, "or" gates, and other logic circuits, in addition to their use as blocking oscillator transformers.

2. THEORY OF OPERATION

2-1. GENERAL

a. The action of a magnetic core can best be described by referring to the drawing of the hysteresis loop (Figure MN-1). The magnetomotive force, or ampere-turns, applied to the winding of a core is measured along the X axis. Magnetic flux density (gausses), or flux lines per square centimeter, is being measured along the Y axis. Once a core has been magnetized and had this magnetization reversed several times, the relationship between flux density and magnetomotive force is described by the hysteresis loop in Figure MN-1.

b. With no current going through any of the core windings, the flux density will be either at point D or at point H, depending upon the direction in which the core has most recently been saturated. If the core is assumed to be at point D on the hysteresis loop and ampere-turns are applied in the negative direction, the relationship between the flux density and the magnetomotive force will follow the line DE. If additional ampere-turns are applied in the negative direction, the core will go on to condition F, at which point saturation has occurred and additional ampere-turns of magnetomotive force will result in only a minor increase in flux level to point G.

c. If the current through the windings is now removed, the core will return to point H on they hysteresis loop. Even though there are no ampere-turns, there is still a flux density proportional to OH in the core. The characteristics of the core material are such that this

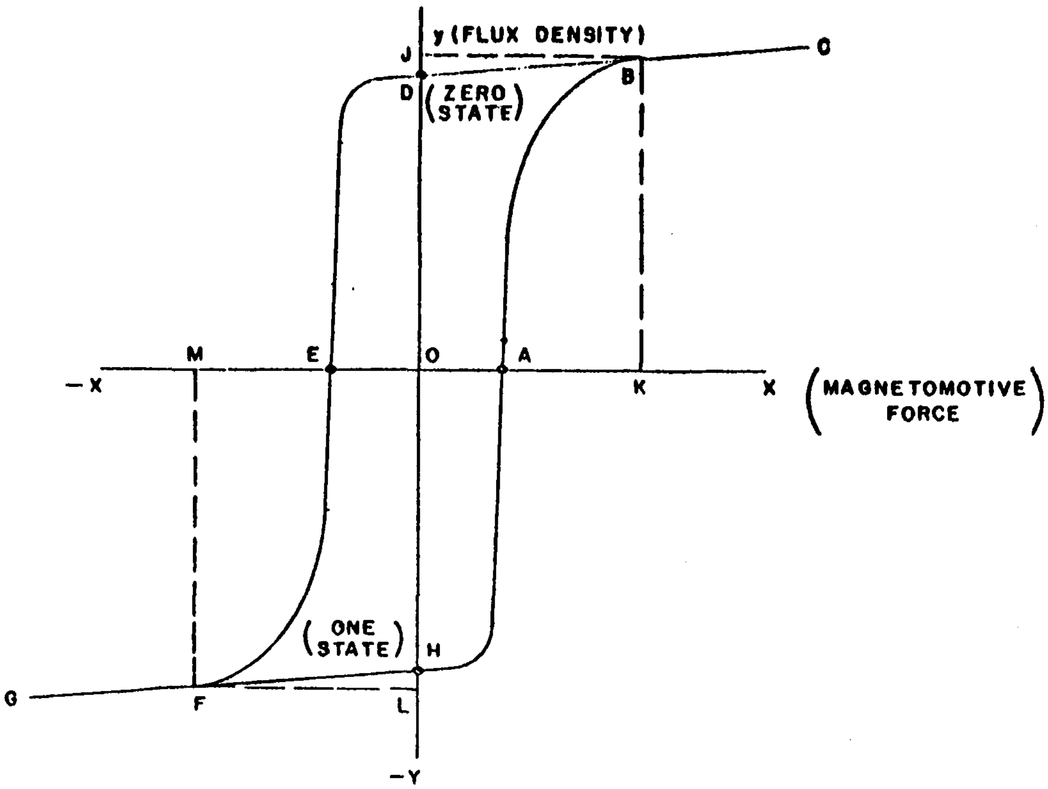


Figure MN-1. Square Hysteresis Loop

flux density will remain indefinitely as though it were a permanent magnetic. If the direction of current in the winding is reversed, positive ampere-turns are applied. This will move the condition of the core from H to A and on to B, at which point the core is now saturated in the positive direction and additional ampere-turns of magnetomotive force will cause very little change in flux density to point C. When the current in the coil is removed, the core will now go from C to D, where it will remain indefinitely until driven again.

d. The net change in flux, when going from a negative quiescent state to plus saturation, is proportional to HJ. It should be noted that other windings on the magnetic core will sense this change in flux and will generate a voltage proportional to the number of turns and the rate of change of flux. Figure MN-2 shows a simple magnetic core with three windings on it. If positive ampere-turns are then applied to winding No. 1, the core condition effectively goes from D to B. Since the hysteresis loop is very square, the change in flux during this time (proportional to DJ) is very small when compared to HJ. As a result, the voltage generated in coil No. 2 will be very small at this time.

e. If negative ampere-turns are again applied so that the core goes from D to E to F, the

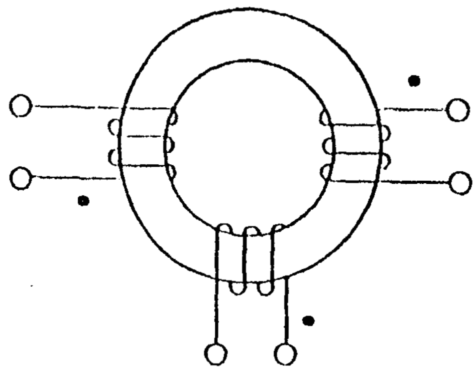


Figure MN-2. Simple Magnetic Core

change in flux will be proportional to DL. The voltage generated in winding No. 2 will now be equal in magnitude, but opposite in polarity, to the voltage generated in that winding when the core went from H to B. These pulses can be separated with diodes and used for different purposes in logic circuits. The two stable states, D and H, are referred to as the "0" state and the "1" state respectively.

2-2. MN11 MAGNETIC CORE

a. A Milgo MN11 magnetic core has four windings and associated components designed specifically for shift register application (Figure MN-3). Pin 7 is connected to a -25v supply. The core drive pulse, applied to pin 1, travels from -25v to approximately zero volts and return, with a rise time no greater than 5 microseconds and a fall time no greater than 10 microseconds. The pulse width must be at least 10 microseconds at 50 percent of measured points, but is normally approximately 40 microseconds wide.

b. This positive going pulse applied to pin 1 results in ampere-turns driving the core beyond positive saturation (Point C in Figure MN-1). When the core drive pulse has passed, the core is left in state D, which is defined as "O" state. The voltage at pin 8 is normally maintained at -25v but is raised to approximately -16v to insert a "1" into the core. It can be seen that the current in the input winding, as a result of a positive going pulse applied to pin 8, will magnetize the core in an opposite direction to that of the drive pulse. The state of the core will go from D to G on the hysteresis loop (Figure MN-1), and when the input pulse is passed, the core remains at H, which is defined as a "1" state.

c. When the next drive pulse occurs, the flux will travel from point H to Point C, and transformer action of the core and windings will result in a positive pulse being generated at the dot end of all four windings. This positive pulse will be approximately 9v in magnitude with a rise time of approximately 6 microseconds. Once the core has gone from negative saturation to positive saturation, there will be no more flux change even though the drive pulse is still present, and no additional voltage is generated in the windings. This switching time, which takes place in approximately 6 microseconds, determines the width of the pulse generated by the windings.

d. The 9v pulse generated in the advance winding causes diode CR3 to conduct, and will charge capacitor C3 to approximately -16v. After the core has switched to positive saturation, the voltage at pin 6 will revert to -25v. Diode CR3, however, prevents capacitor C3 from discharging through the advance winding, so the charge is held on C3 until it discharges through an external load.

e. During a core drive pulse, the voltage at pin 2 jumps from -25v to approximately zero volts because of the IR drop in R1 caused by the shift current. With pin 2 at approximately zero volts, diode CR2 will be reverse biased and no current can flow from pin 8 through CR2 and the input winding. After the core drive pulse has passed, the -16v charge on one CR3 can now discharge through CR2 and the input windings of the next core, driving it to the "1" state. A "1" can be inserted by raising pin 8 to -21v, or more positive. It should be pointed out that a "1" can also be inserted through pin 3, or by applying a pulse to pin 5, which becomes approximately 8v positive with respect to pin 4. If there is no "1" inserted between core drive pulses, the next core drive pulse will drive the core from point D to point C on the hysteresis loop, resulting in a very small change in flux density. This will result in a very small voltage being generated in the windings (approximately 0.5v), giving a signal-to-noise ratio of approximately 18 to 1.

f. It should be noted that energy transferred to a load while shifting out a "1" comes from the core driver and not from the core. The energy in the core merely allows energy to be transferred to the output winding while the core is acting as a transformer. The Milgo MN11 operates equally well on a power supply voltage of -20v instead of -25v as described.

2-3. SHIFT REGISTERS

a. When connected to form a shift register, MN11 cores are connected as shown in Figure MN-3. If a positive going pulse is applied to pin 8 of the first core, a "1" will be inserted into that core. During the next core drive pulse, all of the cores will be pulsed simultaneously, since they are connected in parallel. The resultant 9v pulse from the advance winding of the first core will charge the capacitor in the first core to approximately -16v. When the first core has switched from minus saturation to plus saturation, there will no longer be any voltage generated in the advance winding. CR3 of the first core will prevent the capacitor from discharging through the advance winding, however, and CR2 in the second core prevents this capacitor from discharging through the input winding of the second core. CR2 is reverse biased because of the IR drop in the resistor of the second core caused by the shift current.

g. When the shift pulse has passed, the pin 2 voltage of the second core will go back to -25v and the capacitor in the first core may now discharge through the input winding of the second core. The resultant current through the input winding is sufficient to drive the second core from point D to point G on the saturation curve, so that when C3 is completely discharged, the second core will be in a "1" state. While this second core was being switched from plus saturation to minus saturation, flux linkages were changing in all of the windings of this core, with the result that a voltage was generated in all of these coils with the dot end of the winding negative. Diode CR1 will prevent any current flow in the drive winding as a result of the generated voltage, and the diode CR3 will prevent any current flow in the advance winding as a result of this generated voltage.

h. During the next core drive pulse, core 2 is switched from minus saturation to plus saturation, resulting in the output capacitor of the second core being charged. After the second core drive pulse, the discharge current from this capacitor will insert a "1" into the third core and so on to the last one. Since both ends of the auxiliary winding are brought out, the auxiliary winding may be used to generate either a positive going or negative going 9v pulse. This auxiliary pulse will be approximately 9v in magnitude, with a rise time of six microseconds and a fall time of approximately one half microsecond. In addition, the auxiliary winding can be used to insert "1's" into the core by applying a suitable positive pulse to pin 5 or a suitable negative pulse to pin 4. Pins 2, 3, and 6 are brought out for additional flexibility in adapting the MN11 core to logic circuits.

2-4. BLOCKING OSCILLATORS

a. The use of transformers for blocking oscillators is common and widely understood. It is also possible to use a square loop magnetic core as a blocking oscillator transformer with some desirable results in control of pulse width. Figure MN-4 shows the connections of either an MN12 or an MN13 as used in a blocking oscillator.

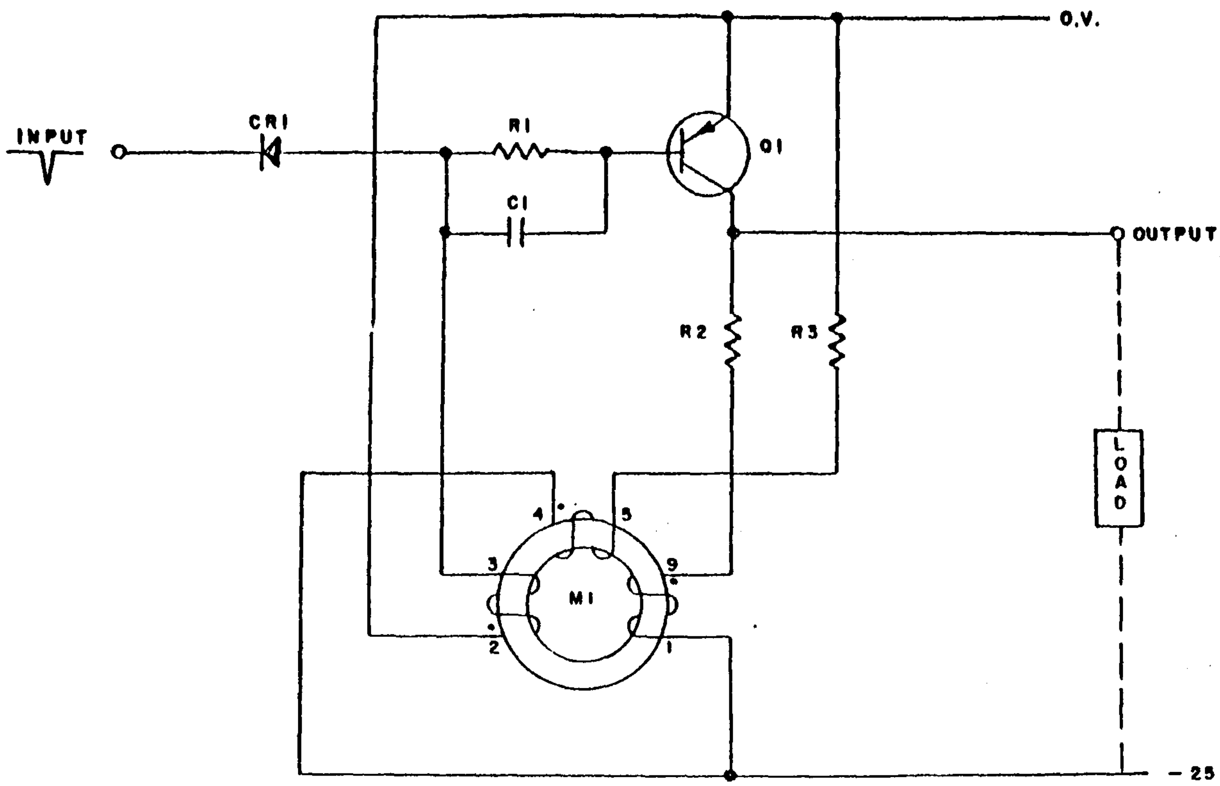


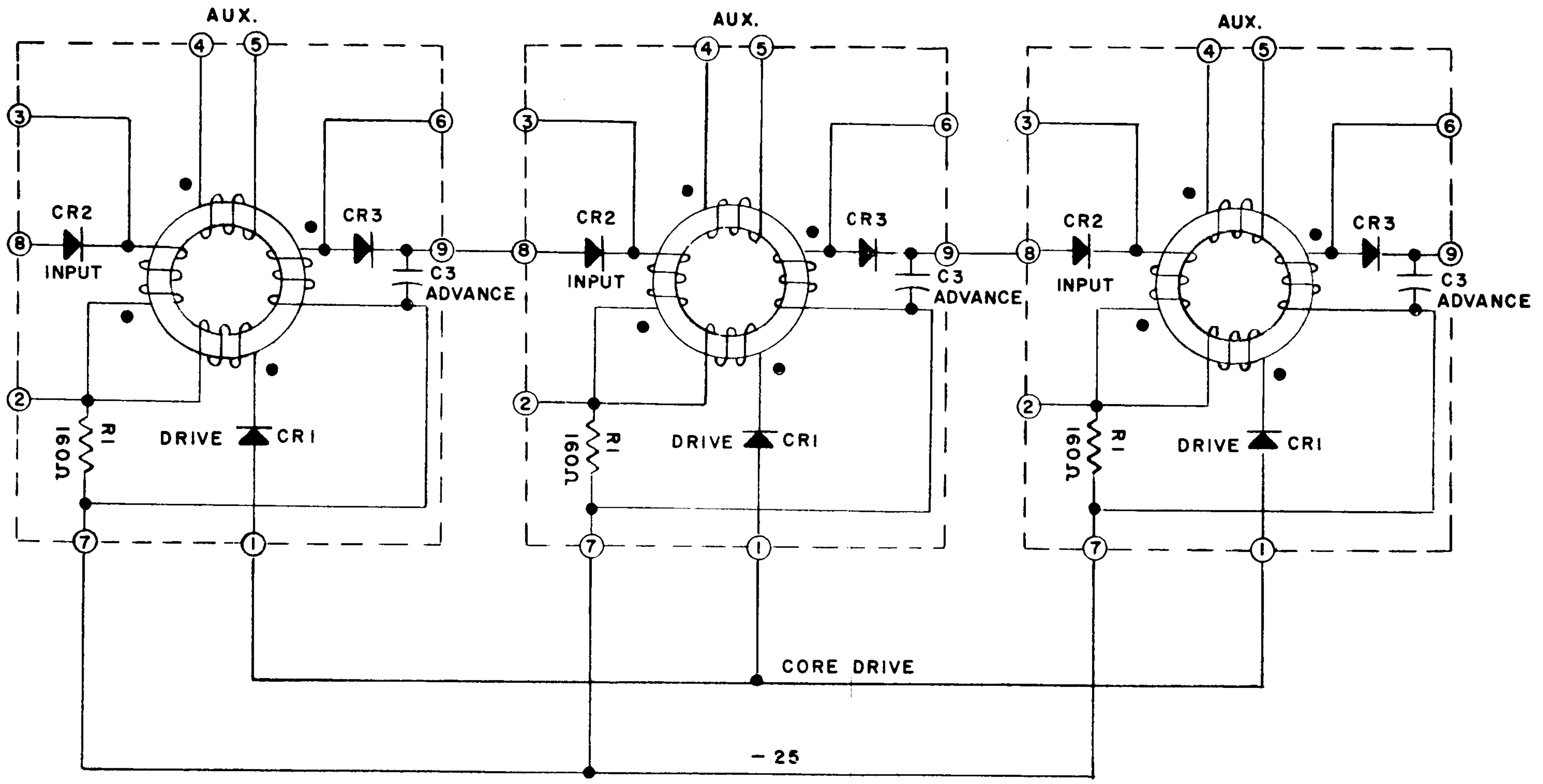
Figure MN-4. Blocking Oscillator (MN12 or MN13)

b. The 9-1 winding is the collector winding and could be compared to the primary winding of a transformer. The 2-3 winding is the feedback winding and could be compared to the secondary winding of a transformer. The 4-5 winding is the reset winding and has no counterpart in a conventional transformer. The reset winding is so connected that the current through the reset winding will drive the core into negative saturation. The transistor will normally be cut off, but when triggered by a negative pulse at the input, will go into conduction. The resulting collector current applies positive ampere-turns to the core and the flux moves from H toward A and B. The resulting flux change in the core is sensed by the feedback winding and a voltage is generated, making pin 3 negative. This negative going voltage is applied to the base of the transistor and drives the transistor into heavier conduction.

c. As the transistor conducts more heavily, the rate of change of flux increases, resulting in an even more negative voltage being applied to the base of the transistor. This feedback very quickly saturates the transistor (approximately one microsecond), but the collector current is limited by resistor R2 and the voltage generated in the collector winding of the core. As long as the core is still in the process of switching from minus saturation to plus saturation, the core and its windings act as a transformer and the feedback winding continues to drive the transistor into saturation. When the core has finally reached saturation (B on hysteresis curve, Figure MN-1), additional ampere-turns from the collector winding will no longer result in a change of flux and no additional voltage will be generated in the feedback winding. This removes the drive to the transistor, which immediately cuts off, removing the ampere-turns from the collector winding.

d. Current through resistor R3 and the reset winding now starts to apply ampere-turns in the negative direction again and drives the core from position D to F. This results in a reversal of flux in the core, which reverses the voltage generated in the feedback winding. Pin 3 now becomes slightly positive, insuring a rapid cutoff of the transistor. Since the duration of the output pulse depends on the time it takes to switch the magnetic core, the pulse width depends on the core used and is relatively independent of the load on the blocking oscillator.

e. Two blocking oscillator cores are used in Milgo equipment: an MN12 and an MN13. The MN12 will cause a pulse approximately 10 microseconds wide to be generated by the blocking oscillator, while the MN'3 will cause a pulse approximately 40 microseconds wide to be generated. It takes approximately 30 microseconds to reset an MN12 core and approximately 80 microseconds to reset an MN13 core.


AUX.
CR2
INPUT
CR3
C3
ADVANCE
R1
160Ω
DRIVE
CR1
CORE DRIVE
- 25